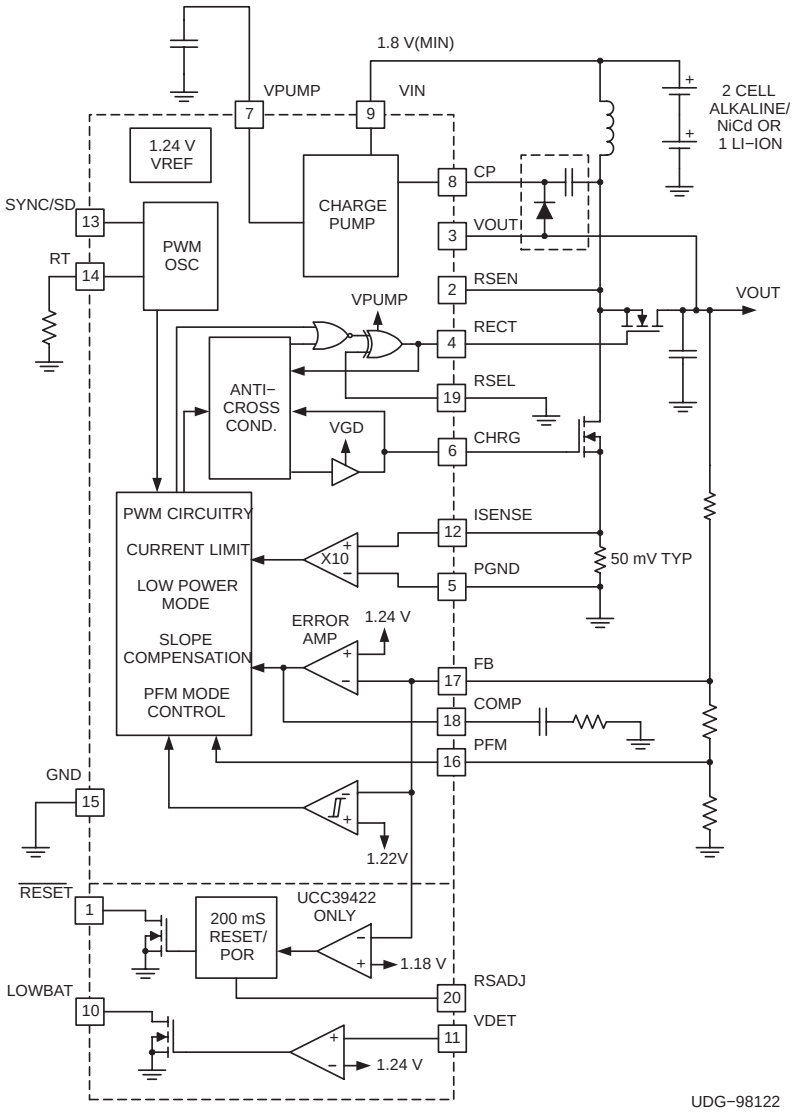
UCC29421, UCC29422, UCC39421, UCC39422
MULTIMODE HIGH-FREQUENCY PWM CONTROLLER

SLUS246C − OCTOBER 1999 − REVISED FEBRUARY 2005

- **Operation Down to an Input Voltage of 1.8 V**
- **High Efficiency Boost, SEPIC or Flyback (Buck-Boost) Topologies**
- **Drives External FETs for High-Current Applications**
- **Up to 2-MHz Oscillator**
- **Synchronizable Fixed Frequency Operation**
- **High-Efficiency Low-Power Mode**
- **High-Efficiency at Very Low-Power with Programmable Variable Frequency Mode**
- **Pulse-by-Pulse Current Limit**
- **5-μA Supply Current in Shutdown**
- **150-μA Supply Current in Sleep Mode**
- **Selectable NMOS or PMOS Rectification**
- **Built-In Power-On Reset (UCC39422 Only)**
- **Built-In Low-Voltage Detect (UCC39422 Only)**

simplified schematic block diagram and application circuit



UDG−98122

description

The UCC39421 family of synchronous PWM controllers is optimized to operate from dual alkaline/NiCd cells or a single Lithium-Ion (Li-Ion) cell, and convert to adjustable output voltages from 2.5 V to 8 V. For applications where the input voltage does not exceed the output, a standard boost configuration is used.

For other applications where the input voltage can swing above and below the output, a 1:1 coupled inductor (Flyback or SEPIC) is used in place of the single inductor. Fixed frequency operation can be programmed, or synchronized to an external clock source. In applications where (at light loads) variable frequency mode is acceptable, the IC can be programmed to automatically enter PFM (pulse frequency modulation) mode for an additional efficiency benefit.

Synchronous rectification provides excellent efficiency at high power levels, where N- or P- type MOSFETs can be used. At lower power levels (between 10% and 20% of full load) where fixed frequency operation is required, low power mode is entered. This mode optimizes efficiency by cutting back on the gate drive of the charging FET. At very low power levels, the IC enters a variable frequency mode (PFM). PFM can be disabled by the user.

description (continued)

Other features include pulse-by-pulse current limiting, and a low 5-μA quiescent current during shutdown. The UCC39422 incorporates programmable power-on reset circuitry and an uncommitted comparator for low voltage detection. The available packages are 20-pin TSSOP or 20-pin N for the UCC39422, and 16-pin TSSOP or 16-pin N for the UCC39421.

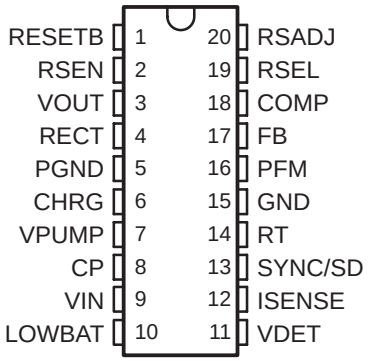
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†‡

Supply Voltage (VIN, VOUT,VPUMP)	8 V
CP	8 V
RSEN	–0.3 V to 12 V
SYNC/SD	–0.3 V to 5 V
ISENSE	–0.3 V to 1 V
Storage Temperature, T_{stg}	–65°C to 150°C
Junction Temperature, T_J	–55°C to 150°C
Lead Temperature (Soldering, 10 seconds)	300°C

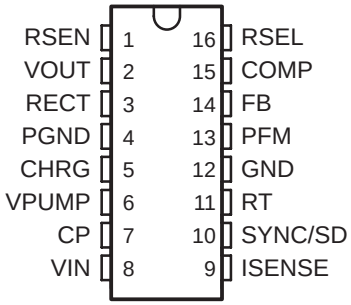
† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltages are with respect to ground. Currents are positive into and negative out of the specified terminals. Consult the Packaging Section of the Databook for thermal limitations and considerations of the package.

TSSOP−20, DIL−20
N, PW PACKAGES
(TOP VIEW)



TSSOP−16, DIL−16
N, PW PACKAGE
(TOP VIEW)



electrical characteristics over recommended operating free-air temperature range, T_A = −40°C to 85°C for the UCC2942x, 0°C to 70°C for the UCC3942x, R_T = 100 kΩ, V_{VPUMP} = 6 V, V_{VIN} = 3 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VIN Section					
Minimum start−up voltage			1.5	1.8	V
Operating current	Not in PFM mode, No load		35	60	µA
Sleep mode current	PFM mode, No load		35	60	µA
Shutdown supply current	SYNC/SD = high		1.5	4	µA
Startup frequency	V_{IN} = 1.8 V	60	120	190	kHz
Startup off time	V_{IN} = 1.8 V		2	5	µs
Startup CS threshold	V_{IN} = 1.8 V		36	56	mV
Minimum PUMP or VOUT voltage to exit startup		2.2	2.5	2.8	V
VPUMP Section					
Regulation voltage	V_{VOUT}=3.3 V, See Note 1	5.0		6.6	V
Operating current	Outputs OFF		100	275	µA
Sleep mode current			5	15	µA
Shutdown supply current	SYNC/SD = High, VOUT = 3 V, V_{VPUMP} = 3 V		2	5	µA
CP voltage to turn-on pump switch	V_{VPUMP} = 5 V		5.3	5.5	V
Pump switch Rds(on)			4		Ω
VOUT Section					
Operating current		300	500	650	µA
Sleep mode current		50	100	150	µA
Shutdown supply current	SYNC/SD = High		1	2.2	µA
VPUMP to VOUT threshold to enable N-channel rectifier	V_{OUT} = 3.3 V	1.4	1.7	2.0	V
Error Amplifier Section					
Regulation voltage	2 V < VIN < 5 V	1.205	1.235	1.265	V
FB input current	V_{FB} = 1.25 V		100	350	nA
Max sinking current, I_{OL}	V_{COMP} = 1 V, V_{FB} = regulation roltage +50 mV	6.5	13	20	µA
Max sourcing current, I_{OH}	V_{COMP} = 0 V, V_{FB} = regulation voltage –50 mV	–20	–13	–6.5	µA
Transconductance	V_{FB} = regulation voltage ±4 mV	150	270	370	µs
Unity gain bandwidth	C_C = 330 pF, See Note 1		100		kHz
Max output voltage	V_{FB} = 0 V	1.6	1.9	2.3	V
Oscillator Section					
Frequency stability	R_T = 350 kΩ	100	150	190	kHz
	R_T = 100 kΩ	375	475	575	kHz
	R_T = 35 kΩ	0.9	1.2	1.4	MHz
R_T voltage		0.600	0.625	0.650	V
SYNC/shutdown threshold		0.9	1.2	1.6	V
SYNC input current	SYNC/SD = 2.5 V			200	nA
Minimum SYNC pulse width	See Note 1			50	ns
Maximum SYNC high time	To avoid shutdown	11	20	29	µs
SYNC range	*f*o = measured frequency at R_T = 100 kΩ	1.1 *f*o		1.7 *f*o	kHz

NOTE 1: Ensured by design. Not production tested.

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PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Sense Section					
Gain		8	10	11	V/V
Overcurrent limit threshold		120	150	190	mV
Unity gain bandwidth	See Note 1		25		MHz
COMP voltage to I_{SENSE} accuracy	I_{SENSE} = 70 mV	0.83	1.00	1.23	V
PWM Section					
Maximum duty cycle	V_{ISENSE} = 0 V, V_{FB} = 0 V	80	88		%
Minimum duty cycle	V_{FB} = 1.5 V			0	%
Low power mode V_{COMP} threshold	At COMP pin	0.53	0.60	0.67	V
Slope compensation accuracy	R_T = 350 kΩ, R_{SLOPE} = 20 kΩ	1.4	2.8	4.0	A/s
Rectifier zero current threshold	RSEL = GND	–2	15	30	mV
	RSEL = VIN	–28	–15	2	mV
RSEL threshold		0.5	0.9	1.3	V
PFM Section					
PFM disable threshold		0.17	0.22	0.27	V
Comp hold during sleep	V_{PFM} = 0.4 V	0.40	0.47	0.65	V
Startup delay after sleep	V_{FB} < 1.23 V		4	9	µs
FB voltage to sleep off		1.185	1.220	1.245	V
VGSW Drive Section					
Rise time	C_O = 1 nF		18	35	ns
Fall time	C_O = 1 nF		14	30	ns
Output high	I_{OUT} = –100 mA, Respect to VPUMP		0.4	0.65	V
	I_{OUT} = –1 mA, Respect to VPUMP		4	10	mV
Output low	I_{OUT} = 100 mA		0.2	0.35	V
	I_{OUT} = 1 mA		2	6	mV
Charge off to rectifier on delay		10	40	65	ns
RECT Drive Section					
Rise time	C_O = 1 nF		20	40	ns
Fall time	C_O = 1 nF		14	30	ns
Output high	I_{OUT} = –100 mA, Respect to VPUMP		0.2	0.5	V
	I_{OUT} = –1 mA, Respect to VPUMP		5	10	mV
Output low rectifier	I_{OUT} = 100 mA		0.2	0.35	V
	I_{OUT} = 1 mA		2	6	mV
Rectifier off to charge on delay		10	40	65	ns
RESET Section (UCC39422 Only)					
Reset timeout	C_{RSADJ} = 0.33 µF	100	250	400	ms
Reset threshold	Percentage below regulation voltage	–7	–5.5	–4	%
Output low voltage	Reset condition, I = 5 mA		0.1	0.25	V
Output leakage	RESET = 8 V		0.05	0.2	µA

NOTE 1: Ensured by design. Not production tested.

electrical characteristics over recommended operating free-air temperature range, T_A = −40°C to 85°C for the UCC2942x, 0°C to 70°C for the UCC3942x, R_T = 100 kΩ, V_{VPUMP} = 6 V, V_{VIN} = 3 V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Voltage Detection Section (UCC39422 Only)					
Threshold voltage		1.18	1.26	1.34	V
Output low voltage	I = 5 mA		0.15	0.3	V
Output leakage	LOWBAT = 8 V		0.05	0.25	µA

PIN DESCRIPTIONS

COMP: This is the output of the transconductance error amplifier. Connect the compensation components from this pin to ground.

CHRG: This is the gate drive output for the N-channel charge MOSFET. Connect it to the gate directly, or through a low-value gate resistor.

CP: This is the input for the charge pump. For applications requiring a charge pump, connect this pin to the charge pump diode and flying capacitor, as shown in the applications diagram of Figure 4. For applications where no charge pump is required, this pin should be grounded.

FB: The feedback input is the inverting input to the transconductance error amplifier. Connect this pin to a resistive divider between V_{OUT} and ground. The output voltage is regulated to:

$$V_{OUT} = 1.235 \times \frac{(R1 + R2)}{R1}$$

where R1 goes to GND and R2 goes to VOUT.

GND: This is the signal ground pin for the device. It should be tied to the local ground plane.

ISENSE: This is the input to the X10 wide bandwidth current-sense amplifier. Connect this pin to the high side of the current-sense resistor. An internal current is sourced out this pin for slope compensation. For applications requiring slope compensation (or filtering of the current-sense signal), use a resistor in series with this pin.

LOWBAT: This is the open drain output of the uncommitted comparator. (UCC39422 only). This output is low when the VDET pin is above 1.25 V.

PFM: This is the programming pin for the PFM (pulse frequency modulation) mode threshold. Connect this pin to a resistive divider off of the FB pin (or VOUT) to set the PFM threshold. To disable PFM Mode, connect this pin to ground (below 0.2 V).

PGND: This is the power ground pin for the device. Connect it directly to the ground return of the current-sense resistor.

RECT: This is the gate drive output for the synchronous rectifier. Connect it to the gate of the P- or N-channel MOSFET directly, or through a low value gate resistor.

RSEN: This pin is used to sense the voltage across the synchronous rectifier for commutation. In boost configurations, connect this pin through a 1-kΩ resistor to the junction of the two MOSFETs and the inductor. In flyback and SEPIC configurations, connect this pin through a 1-kΩ resistor to the junction of the drain of the synchronous rectifier and the secondary side winding of the coupled inductor.

RSADJ: A capacitor from this pin to ground sets the reset delay. (UCC39422 only)

RSEL: This pin programs the device for N- or P-channel synchronous rectifiers by inverting the phase of the RECT gate drive output. Connect this pin to ground for N-channel MOSFETs, connect it to V_{IN} for P-channel MOSFETs.

$\overline{\text{RESET}}$: This is the open drain output of the reset comparator. (UCC39422 only) and is active low.

RT: A resistor from this pin to ground programs the frequency of the pulse width modulator.

$$\text{Frequency (MHz)} \cong \frac{50}{R_T\ (k\Omega)}$$

SYNC/SD: This pin has two functions. It may be used to synchronize the UCC39421's switching frequency to an external clock, or to shutdown the IC entirely. In shutdown, the quiescent current is reduced to just a few microamps (both external FETs are turned off). To shutdown the converter, this pin must be held high (above 2.0 V) for a minimum of 29 μs. If not used, this pin should be grounded.

To synchronize the internal oscillator to an external source, the SYNC/SD pin must be driven with a clock pulse, with a minimum amplitude of 2.0 V. The internal circuitry syncs to the rising edge of the external clock. The clock pulse width is not critical (must be 50 ns minimum).

Note: When coming out of shutdown (or during power-up), the SYNC/SD pin must be held low for a minimum of 200 μs before applying an external clock to ensure startup.

VPUMP: This is the output of the charge pump. For applications requiring a charge pump, connect a 1-μF capacitor from this pin to ground. Otherwise, connect this pin to the higher of V_{IN} or V_{OUT}, and decouple with a 0.1-μF capacitor.

VOUT: Connect this pin to the output voltage. This input is used for sensing the voltage across the synchronous rectifier and for supplying power to internal circuitry and should be decoupled with a 0.1-μF capacitor.

VIN: This is the input power pin of the device. Connect this pin to the input voltage source. A 0.1-μF decoupling capacitor should be connected between this pin and ground.

VDET: This is the non-inverting input to an uncommitted comparator. This input may be used for detecting a low-battery condition. (UCC39422 only)

APPLICATION INFORMATION

The UCC39421 is a high frequency, synchronous PWM controller optimized for portable, battery-powered applications where size and efficiency are of critical importance. It includes high-speed, high-current FET drivers for those converter applications requiring low Rds(on) external MOSFETs. A detailed block diagram is shown in Figure 2.

optimizing efficiency

The UCC39421 optimizes efficiency and extends battery life with its low quiescent current and its synchronous rectifier topology. The additional features of low-power (LP) mode and PFM mode maintain high efficiency over a wide range of load current. These features are discussed in detail.

power saving modes

Since this is a peak current mode controller, the error amplifier output voltage sets the peak inductor current required to sustain the load. The UCC39421 incorporates two special modes of operation designed to optimize efficiency over a wide range of load current. This is done by comparing the error amplifier output voltage (on the COMP pin) to two fixed thresholds (one of which is user programmable). If the error amplifier output voltage drops below the first threshold, low power mode is entered. If the error-amplifier output voltage drops even further, below a second user programmable threshold, PFM mode is entered. These modes of operation are designed to maintain high efficiency at light loads, and are described in detail in the following text. Refer to the simplified block diagram of Figure 1 for the control logic.

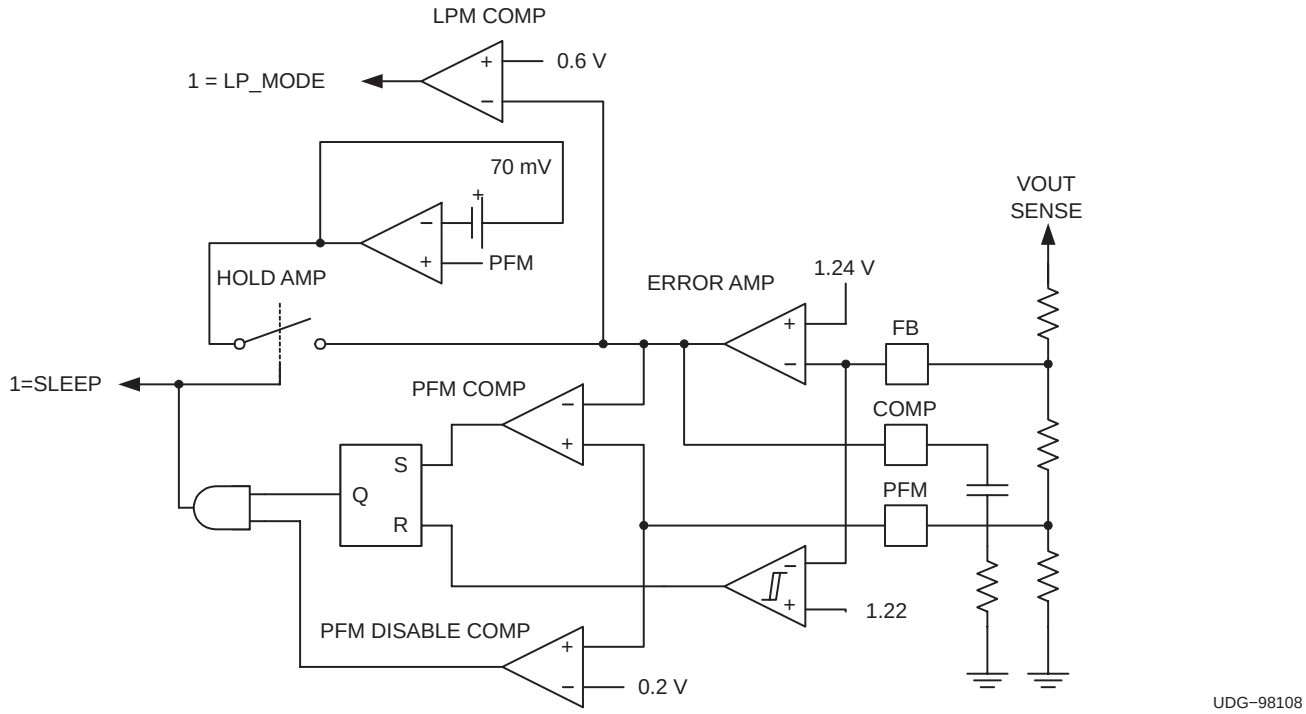

Figure 1. Simplified Block Diagram of Low Power and Pulse Mode Control Logic

APPLICATION INFORMATION

power saving modes (continued)

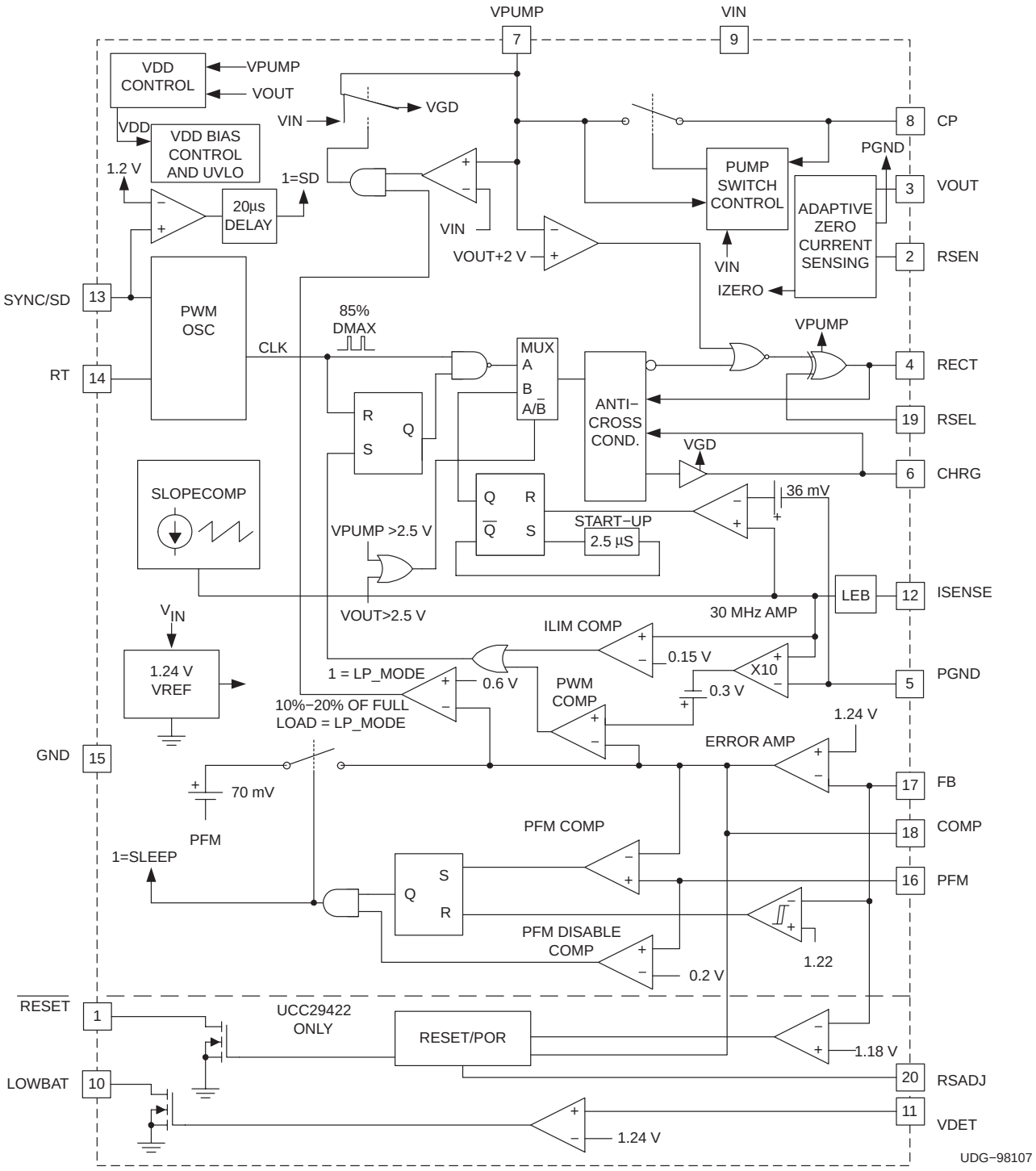

Figure 2. Detailed Block Diagram

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low power mode

During normal operation, at medium to high load currents, the switching frequency remains fixed, programmed by the resistor on the RT pin. At these higher loads, the gate drive output on the CHRG pin (for the N-channel charge FET) is the higher of V_{IN} or V_{PUMP}. When the load current drops (sensed by a drop in the error amp voltage), the UCC39421 automatically enters LP mode, and the gate drive voltage on the CHRG pin is reduced to lower gate drive losses. This helps to maintain high efficiency at light loads where the gate drive losses begin to dominate and the lowest possible Rds(on) is not required. If the load increases, normal or “high power” mode resumes. The expression for gate drive power loss is given by equation (1). It can be seen that the power varies as a function of the applied gate voltage squared.

$$P_{GATELOSS} = \frac{Q_G \times \left(V_G\right)^2 \times f}{V_S} \quad (1)$$

Where Q_G is the total gate charge and V_S is the gate voltage specified in the MOSFET manufacturer’s data sheet, V_G is the applied gate drive voltage, and f is the switching frequency.

The nominal COMP voltage where LP mode is entered is 0.6 V. Given the internal offset and gain of the current-sense amplifier, this corresponds to a peak switch current of:

$$I_{PEAK} = \frac{(0.6 - 0.3)}{K \times R_{SENSE}} = \frac{0.03}{R_{SENSE}} \quad (2)$$

Where 0.6 V is the threshold for LP mode, 0.3 V is the internal offset, K is the nominal current-sense amplifier gain of 10, and R_{SENSE} is the value of the current-sense resistor. If the peak inductor current is below this value, the UCC39421 enters LP mode and the gate drive voltage on the CHRG pin is equal to V_{IN}. At peak currents higher than this, the gate drive voltage is the higher of VIN or VPUMP.

PFM mode

At very light loads, the UCC39421 enters PFM mode. In this mode, when the error amplifier output voltage drops below the PFM threshold, the controller goes into sleep mode until V_{OUT} has dropped slightly (30 mV measured at the feedback pin). At this time, the controller turns back on and operates at fixed frequency for a short duration (typically a few hundred microseconds) until the output voltage has increased and the error amplifier output voltage has dropped below the PFM threshold once again. Then the converter turns off and the cycle repeats. This results in a very low duty cycle of operation, reducing all losses and greatly improving light load efficiency. During sleep mode, most of the circuitry internal to the UCC39421 is powered down, reducing quiescent current and maximizing efficiency.

The peak inductor current at which this mode is entered is user programmable by setting the voltage on the PFM pin. This can be done with a single resistor in series with the feedback divider, as shown in the application diagrams. The nominal peak current threshold for PFM mode is defined by the equation:

$$I_{PEAK} \cong \frac{\left(\frac{1.25 \times R1}{(R1 + R2)}\right) - 0.3}{K \times R_{SENSE}} \quad (3)$$

APPLICATION INFORMATION

PFM mode (continued)

Where 0.3 V is the internal offset and K is the nominal current-sense amplifier gain of 10 and R_{SENSE} is the value of the current-sense resistor. Note that in this case, the PFM pin voltage is set by the R1/R2 resistive divider off of the FB pin, which is regulated to 1.25 V.

During sleep mode, the COMP pin is forced to 70 mV above the PFM pin voltage. This minimizes error amplifier overshoot when coming out of sleep mode, and prevents erroneously tripping the PFM comparator.

disabling PFM mode

The user may disable PFM mode by pulling the PFM pin below 0.2 V. In this case, the UCC39421 remains on, in fixed frequency operation at all load currents. The PFM pin can also be driven, through a resistive divider, off of an output from the system controller. This allows the system controller to prepare for an expected step increase in load, improving the converter's large signal transient response. An example of this is shown in Figure 3.

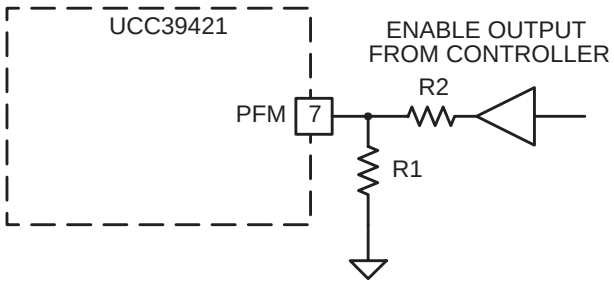

Figure 3. Driving the PFM Pin From a Controller Output

choosing a topology and optimal synchronous rectifier

The UCC39421 is designed to be very flexible, and can be used in boost, flyback and SEPIC topologies. It can operate from input voltages between 1.8 V and 8.0 V. Output voltages can be between 2.5 V and 8.0 V. It can also drive either N- or P-channel MOSFET synchronous rectifiers. Table 1 can be used to select the appropriate topology for a given combination of input and output voltage requirements. Although it is designed to operate as a peak current mode controller, it can also be configured for voltage mode control. This is discussed in a later section.

The user can program the gate drive output on the RECT pin for N-channel MOSFETs by grounding the RSEL pin, or for P-channel MOSFETs by connecting the RESEL pin to VIN. Table 2 is used to determine whether an N- or P-channel synchronous rectifier should be used.

***Note**: In all cases, low-voltage-logic MOSFETs should be used to achieve the lowest possible on-resistance for the highest efficiency.*

The application diagrams in Figures 4 through 8 illustrate the use of the UCC39421 in all the topologies, using N- and P-channel rectifiers. They are be discussed in detail in the next section.

APPLICATION INFORMATION

choosing a topology and optimal synchronous rectifier (continued)

Note that the higher the frequency of operation, the more critical the MOSFET gate charge becomes for efficiency, particularly at light loads. However, high load currents demand lower Rds(on), which tends to increase gate charge. These two parameters should be balanced. At lower frequencies, the gate charge becomes less important, at 1 MHz or more, it is critical.

Table 1. SELECTING TOPOLOGY BASED ON INPUT AND OUTPUT VOLTAGE REQUIREMENTS

Cell Type	Nunber of Cells	V_{IN} Range	V_{OUT}	Topology
Alkaline or NiCd, NiMH	2	1.8 V to 3.0 V	3.0 < V < 8.0	Boost
	3	2.7 V to 4.5 V	2.5 < V < 3.9	Flyback or SEPIC
			4.5 < V < 8.0	Boost
			V > 8.0	Non−synchronous boost
Li-Ion	1	2.5 V to 4.2 V	2.5 < V < 3.6	Flyback or SEPIC
			4.2 < V < 8.0	Boost
			V > 8.0	Non−synchronous boost

boost topology

The boost topology is simple and efficient, and should be used whenever the desired output voltage is greater than the maximum input voltage.

boost using two n-channel MOSFETs

A boost converter using two N-channel MOSFETs is shown in Figure 4. This configuration is optimal for output voltages below 4 V, where the output voltage may not be high enough to provide optimal gate drive for a P-channel MOSFET. Note that in this case, a charge pump is required to provide proper gate drive levels. This is easily accomplished by adding an external diode and a capacitor, as shown. The diode connects from the output voltage to the CP pin. It should be an ultrafast or a Schottky diode. A 0.1-µF ceramic capacitor is connected from the drain of the charge FET to the CP pin. This is the “flying” capacitor that charges to (V_{OUT} – V_{DIODE}) every time the charge FET is on. A charge pump reservoir capacitor is connected from the VPUMP pin to ground. It should be at least 1µF. A high-speed active rectifier inside the UCC39421 charges the pump capacitor from the CP pin. The charge pump voltage is:

$$V_{PUMP} \cong 2 \times V_{OUT} \quad (4)$$

For a block diagram of the charge pump logic, refer to Figure 12.

***Note**: A charge pump should not be used at output voltages over 4.0 V to avoid pump voltages exceeding 8 V.*

For other applications, where the charge pump is not required, the CP pin should be grounded and the pin should be connected to either V_{OUT} or V_{IN}, whichever is greater.

APPLICATION INFORMATION

boost using two n-channel MOSFETs

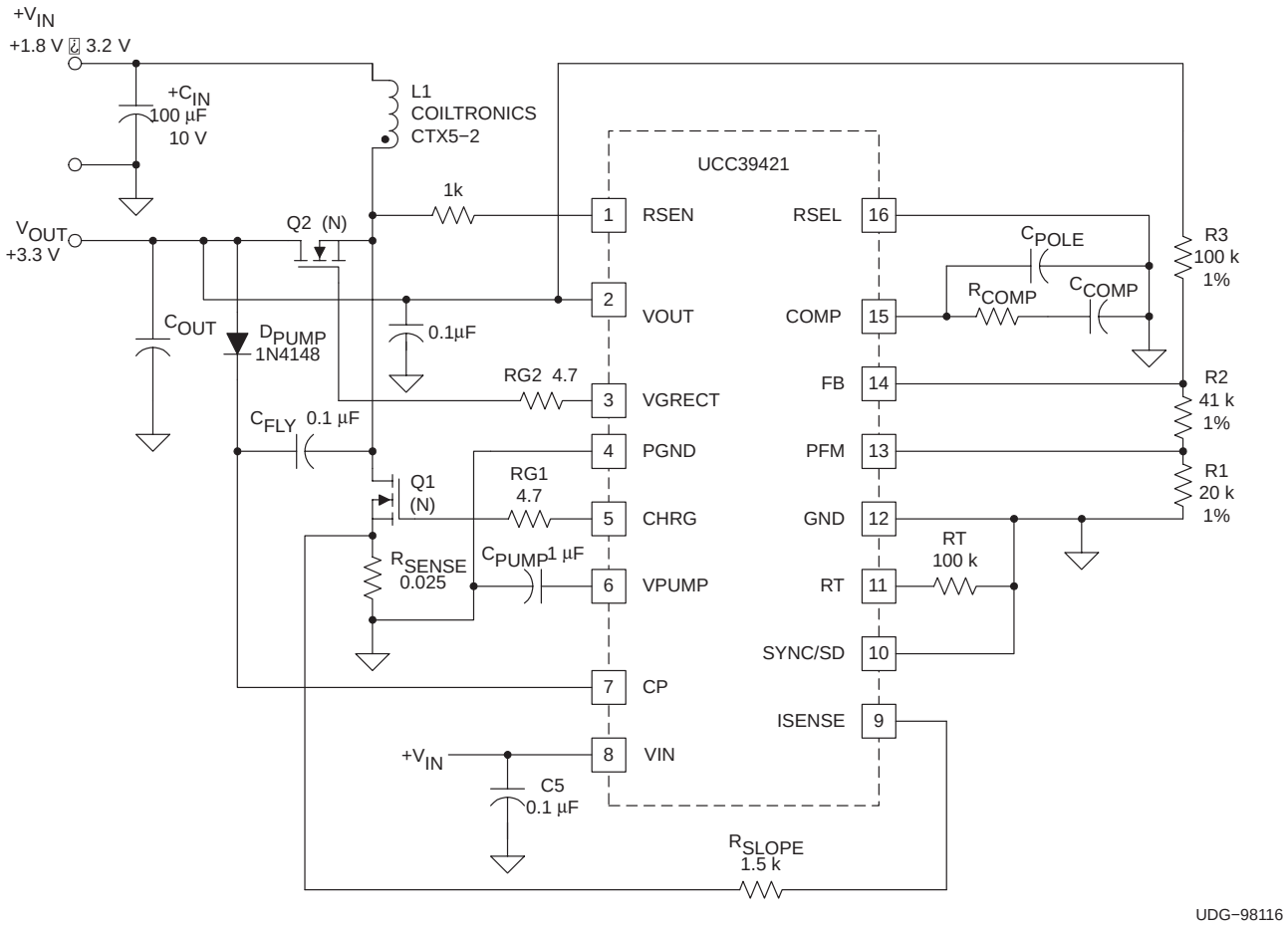

Figure 4. Application Diagram for the Boost Topology Using the N-channel Synchronous Rectifier

Table 2. SELECTING SYNCHRONOUS RECTIFIER BASED ON TOPOLOGY AND OUTPUT VOLTAGE

Topology	V_{OUT}	Synchronous Rectifier
Boost	3.0 < V < 8.0	P-channel (low voltage logic)
	V < 4.0	N-channel (low voltage logic) *Note: Requires a diode and a capacitor for the charge pump*
	V > 8.0	Non-synchronous *Note: Use Schottky rectifier (See Figure 16)*
Flyback	2.5 < V < 3.0	N-channel (low voltage logic) *Note: Requires a diode and a capacitor for the charge pump*
	3.0 < V < 8.0	N-channel (low voltage logic)
SEPIC	3.0 < V < 8.0	P-channel (low voltage logic)

APPLICATION INFORMATION

boost using N- and P-channel MOSFETs

For output voltages greater than the input and greater than about 3.0 V, a P-channel may be used for the synchronous rectifier. This configuration is shown in Figure 5. In this case, the VPUMP pin should be connected to VOUT. This configuration can be used for a 3.3 V output if a low voltage logic MOSFET is used.

relating peak inductor current to average output current for the boost converter

For a continuous mode boost converter, the average output current is related to the peak inductor current by the following:

$$I_{PEAK} = \left(\frac{I_{OUT}}{(1 - D)}\right) + \frac{di}{2} \quad (5)$$

where D is the duty cycle and the inductor ripple current, di, is defined as:

$$di = \frac{t_{ON} \times V_{IN}}{L} = \frac{D \times V_{IN}}{f \times L} \quad (6)$$

where f is the switching frequency and L is the inductor value. The duty cycle is defined as:

$$D = \left(\frac{V_O - V_{IN}}{V_O}\right) \quad (7)$$

Substituting equations (6) and (7) into equation (5) yields:

$$I_{PEAK} = \frac{I_{OUT}}{\left(1 - \left(\frac{V_O - V_{IN}}{V_O}\right)\right)} + \frac{V_{IN}}{2 \times f \times L} \times \left(\frac{V_O - V_{IN}}{V_O}\right) \quad (8)$$

Note that in these equations, the voltage drop across the rectifier has been neglected.

APPLICATION INFORMATION

relating peak inductor current to average output current for the boost converter

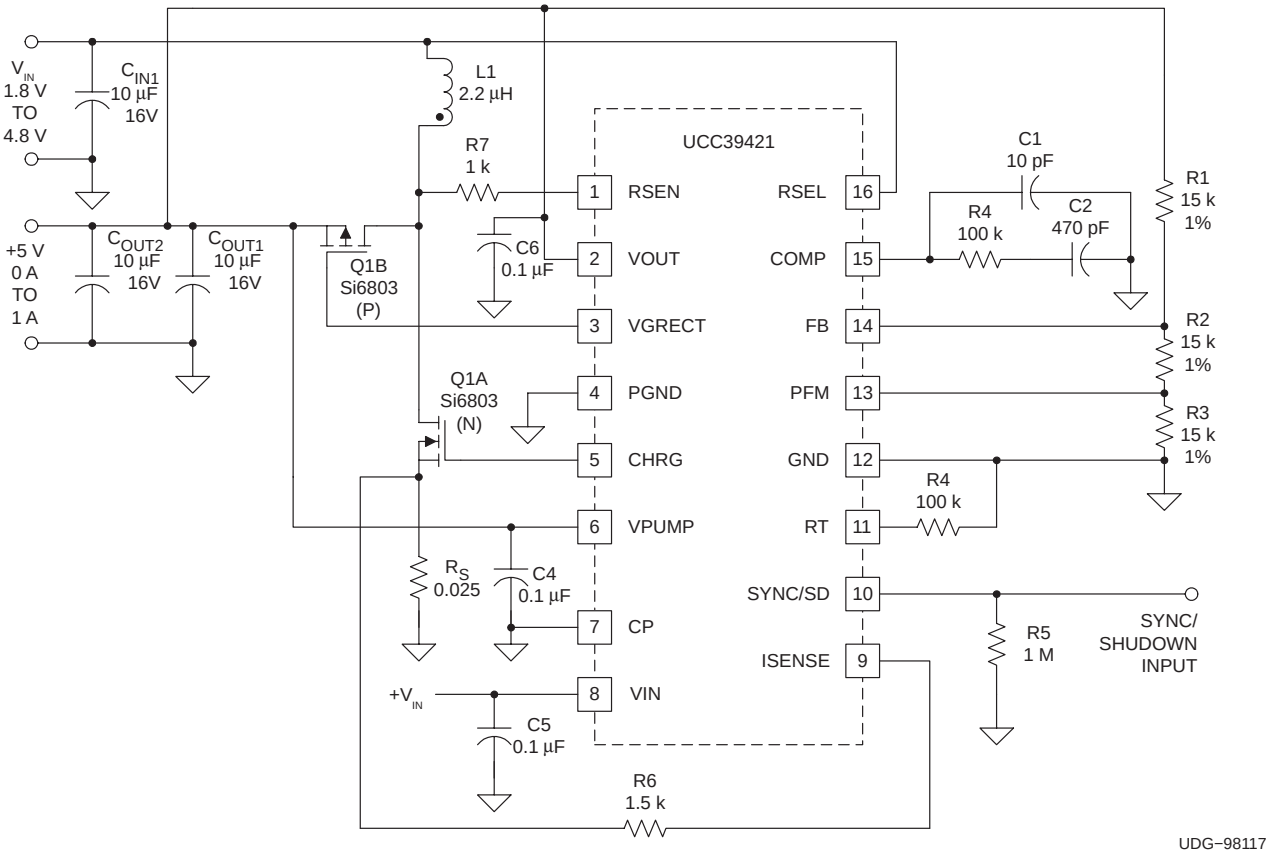

Figure 5. Application Diagram for the Boost Topology Using a P-channel Synchronous Rectifier

flyback topology using n-channel MOSFETs

A flyback converter using the UCC39421 is shown in Figure 6. It uses a standard two-winding coupled inductor with a 1:1 turns ratio. The advantage of this topology is that the output voltage can be greater or less than the input voltage, as shown in Table 1. For example, this is ideal for generating 3.3 V from a Lithium-Ion cell. Note that RC snubbers are placed across the primary and secondary windings to reduce ringing due to leakage inductance. These are optional, and may not be required in the application.

Note that for converters where V_{IN} and V_{OUT} may both be below 3 V, a charge pump is needed to provide adequate gate drive. This is illustrated in the example if Figure 7.

APPLICATION INFORMATION

flyback topology using n-channel MOSFETs (continued)

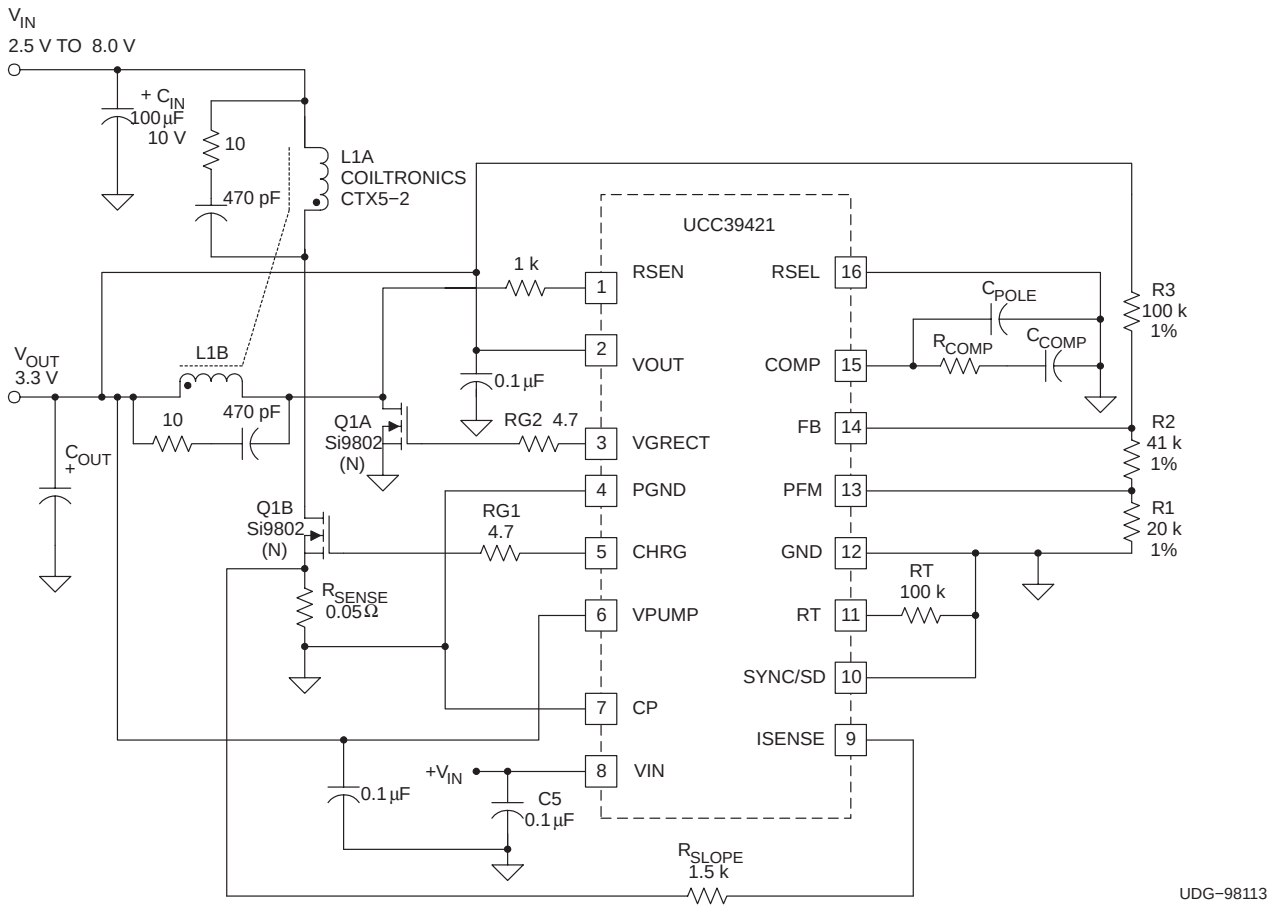

Figure 6. Application Diagram for the Flyback Topology Using the N-channel Synchronous Rectifier

APPLICATION INFORMATION

flyback topology using n-channel MOSFETs (continued)

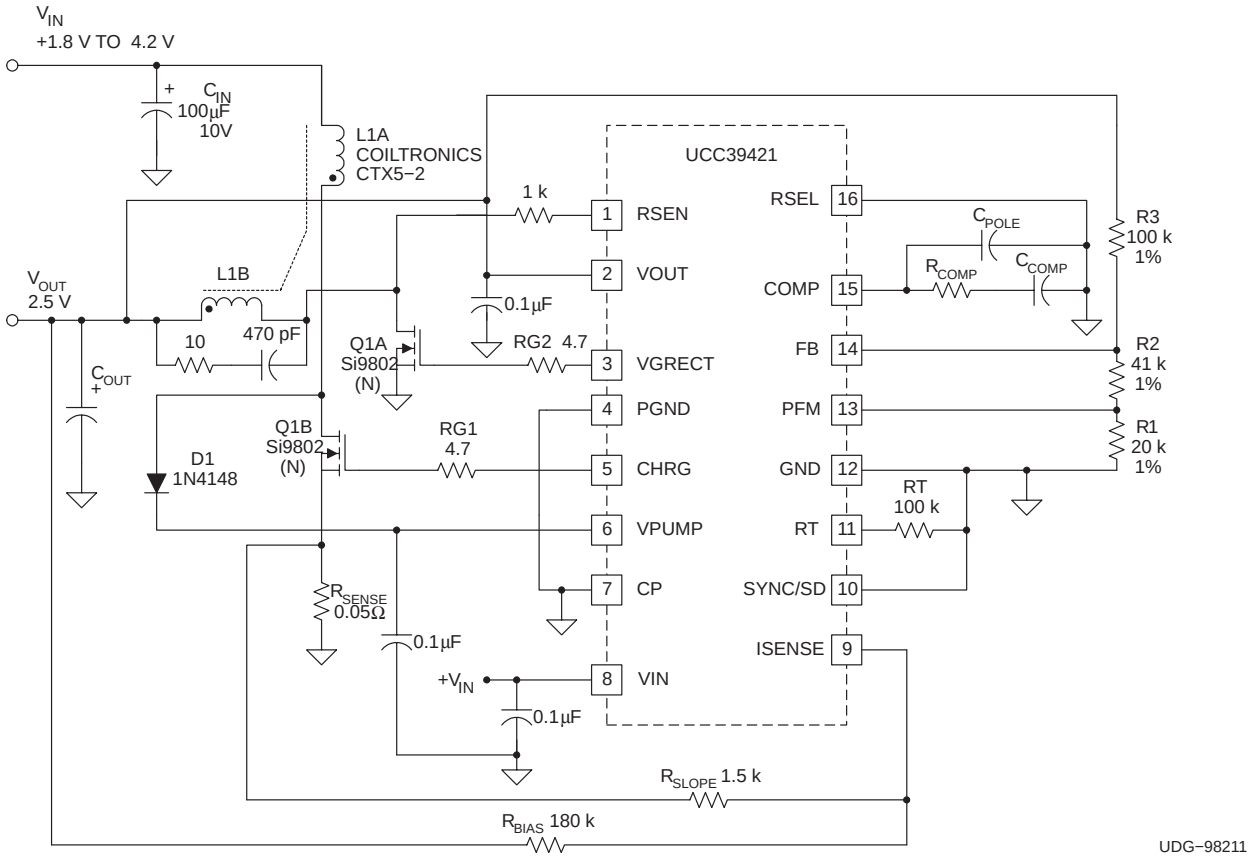

Figure 7. Flyback Converter Using Charge Pump Input for Low Voltage Operation

relating peak inductor current to average output current for the flyback converter

For a continuous mode flyback converter, the average output current is related to the peak inductor current by the following:

$$I_{PEAK} = \left(\frac{I_{OUT}}{(1 - D)} \right) + \frac{di}{2} \tag{9}$$

where D is the duty cycle and the inductor ripple current, dI, is defined as:

$$di = \frac{t_{ON} \times V_{IN}}{L} = \frac{D \times V_{IN}}{f \times L} \tag{10}$$

where f is the switching frequency and L is the inductor value. The duty cycle is defined as:

APPLICATION INFORMATION

relating peak inductor current to average output current for the flyback converter (continued)

$$D = \left(\frac{V_O}{V_{IN} + V_O} \right) \tag{11}$$

Substituting equations (10) and (11) into equation (9) yields:

$$I_{PEAK} = \frac{I_{OUT}}{\left(1 - \left(\frac{V_O}{V_{IN}+V_O}\right)\right)} + \frac{V_{IN}}{2 \times f \times L} \times \left(\frac{V_O}{V_{IN} + V_O} \right) \tag{12}$$

Figure 7 shows an example of a converter where both V_{IN} and V_{OUT} may be quite low in voltage. In this case, a diode has been added to peak detect the voltage on the drain of the charge FET and use it for the pump input voltage. This is used to drive the gates of the FETs. To assure that the pump voltage is used (rather than V_{IN}, which may be low), resistor R_{BIAS} has also been added to the ISENSE input to inhibit LP mode. This technique is discussed further in the section *Changing the Low Power Threshold*.

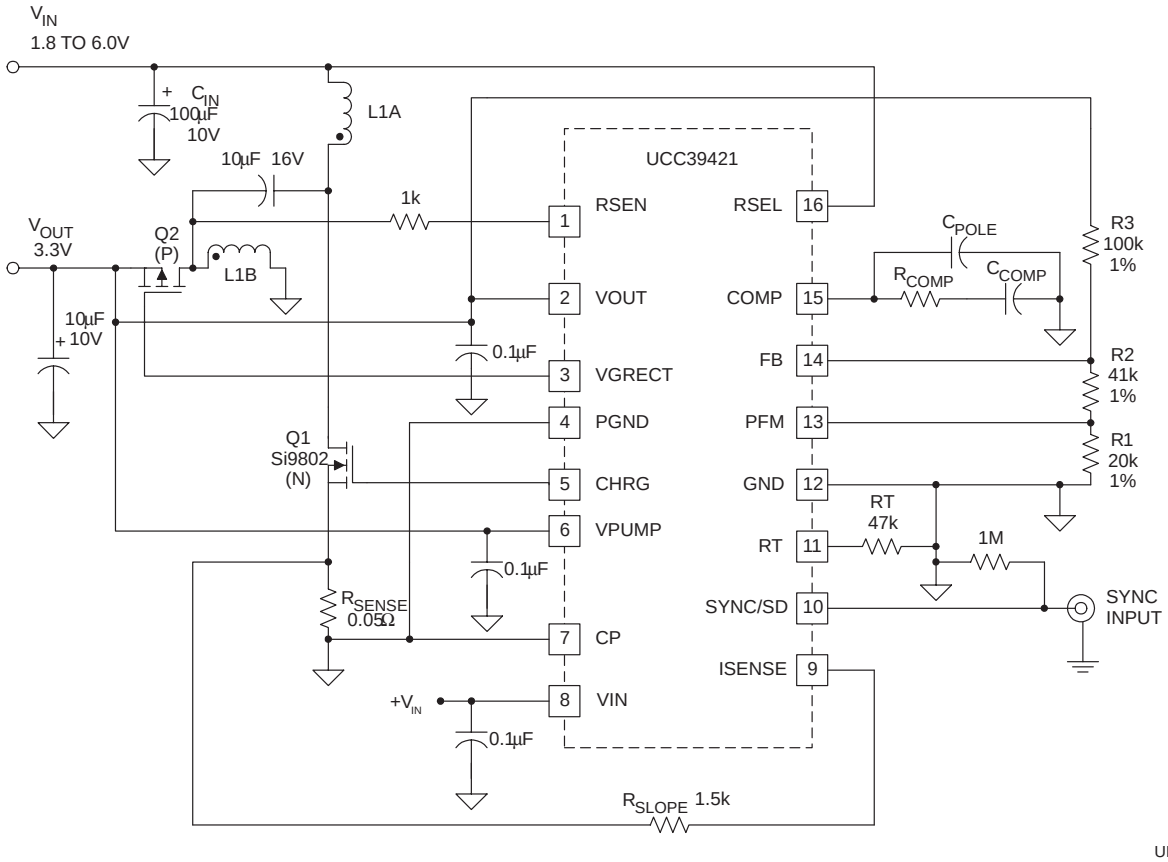

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Figure 8. Application Diagram for the SEPIC Technology Using a P-channel Synchronous Rectifier

APPLICATION INFORMATION

SEPIC topology using N- and P-channel MOSFETs

The UCC39421 may also be used in the SEPIC (single-ended primary inductance converter) topology. This topology, which is similar to the flyback, uses a capacitor to aid in energy transfer from input to output. This configuration is shown in Figure 8. The N-channel synchronous rectifier has been changed to a P-channel and moved to the other end of the inductor's secondary winding, and a new capacitor has been placed across the dotted ends of the two windings. The SEPIC topology offers the same advantage of the flyback in that it can generate an output voltage that is greater or less than the input voltage.

However, it also offers improved efficiency. Although it requires an additional capacitor in the power stage, it greatly reduces ripple current in the input capacitor and improves efficiency by transferring the energy in the leakage inductance of the coupled inductor to the output. This also provides snubbing for the primary and secondary windings, eliminating the need for RC snubbers. Note that the capacitor must have low ESR, with sufficient ripple current rating for the application. Another advantage of the SEPIC is that the inductors do not have to be on the same core.

PWM duty cycle and slope compensation

All boost and flyback converters using peak current mode control are susceptible to a phenomenon known as subharmonic oscillation when operated in the continuous conduction mode beyond 50% duty cycle. Continuous conduction mode (CCM) means that the inductor current never goes to zero during the switching cycle. For a CCM boost converter, the required duty cycle for a given input and output voltage (neglecting voltage drops across the MOSFET switches) is given by equation (7). This is shown graphically for a number of common output voltages in Figure 9. For example, it can be seen that for a 3.3-V output (using the boost topology) slope compensation is not required because the duty cycle never exceeds 50%.

For the flyback topology, using a coupled inductor with a 1:1 turns ratio, the duty cycle is defined by equation (11). This is shown graphically for a number of common output voltages in Figure 10.

To prevent subharmonic oscillation beyond 50% duty cycle, a technique called slope compensation is used, which modifies the slope of the current ramp. This is accomplished by adding a part of the timing ramp to the current-sense input. In the UCC39421, this can be done by simply adding a resistor in series with the ISENSE input. A current is sourced within the IC which is proportional to the internal timing ramp voltage. The value of the resistor determines the amount of slope compensation added.

The slope compensation output current at the ISENSE pin is equal to:

$$I_{SLOPE} = \frac{1}{R_T} A/\mu sec \tag{13}$$

where RT is the timing resister in ohms (Ω).

The required slope compensation resistor for a boost configuration is given by the equation:

$$R_{SLOPE} = \frac{\left(V_{OUT} - 2 \times V_{IN(min)}\right) \times R_{SENSE} \times R_T}{L} \tag{14}$$

where R_{SENSE} is the current-sense resistor value in ohms (Ω) and L is the inductor value in microhenries (μH).

APPLICATION INFORMATION

PWM duty cycle and slope compensation (continued)

For a flyback topology, using a 1:1 turns ratio, the equation becomes:

$$R_{SLOPE} = \frac{\left(V_{OUT} - V_{IN(min)}\right) \times R_{SENSE} \times R_T}{L} \quad (15)$$

If the converter is operated in the discontinuous conduction mode (inductor current drops to zero), no slope compensation is required. The point at which this mode boundary occurs is a function of switching frequency, input voltage, output voltage, load current, and inductor value. However, in general the converter is more efficient when operated in the continuous conduction mode due to the lower peak currents.

CCM BOOST CONVERTER DUTY CYCLE vs INPUT VOLTAGE

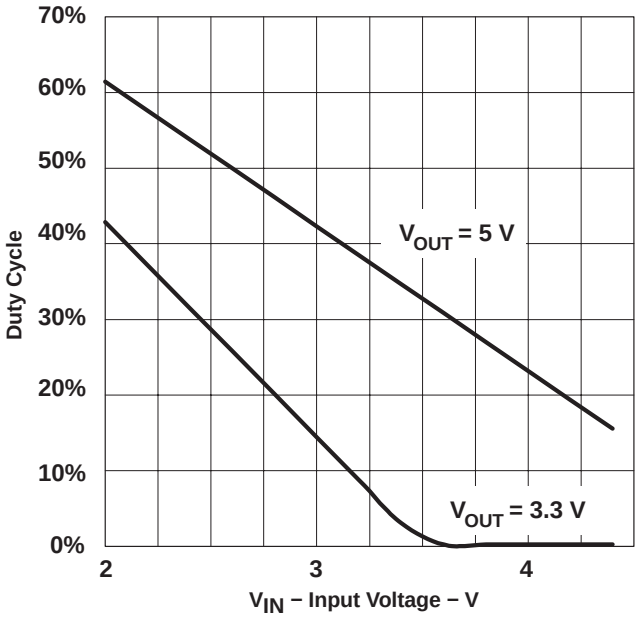


Figure 9

CCM FLYBACK CONVERTER DUTY CYCLE vs INPUT VOLTAGE

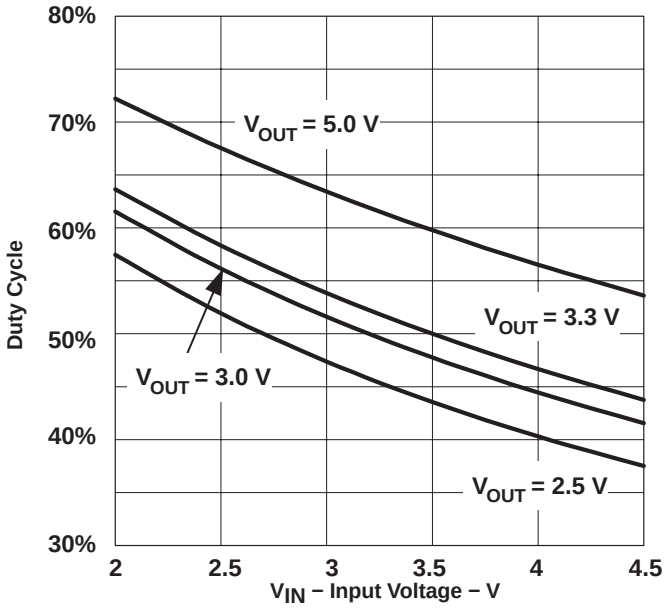


Figure 10

voltage mode control

The UCC39421 can be operated as a voltage mode controller by connecting a 5.6-kΩ resistor from the ISENSE pin to ground. The internal current source generates an artificial ramp voltage on this input. In this case, no slope compensation is required, and no current-sense resistor is required in series with the source of the N-channel MOSFET. A typical application diagram is shown in Figure 11. However, in this configuration there is no overcurrent protection. In addition, the pulse and low power modes, designed to increase efficiency at light loads, operates at different load currents. This is because the internal error amplifier's output voltage is no longer a direct function of load current, but rather of duty cycle. When operating in CCM, the duty cycle is largely a function of input and output voltage, not load current. At light enough loads however, the converter goes into discontinuous mode and the error amplifier voltage drops low enough to activate the low power and pulse modes.

APPLICATION INFORMATION

voltage mode control (continued)

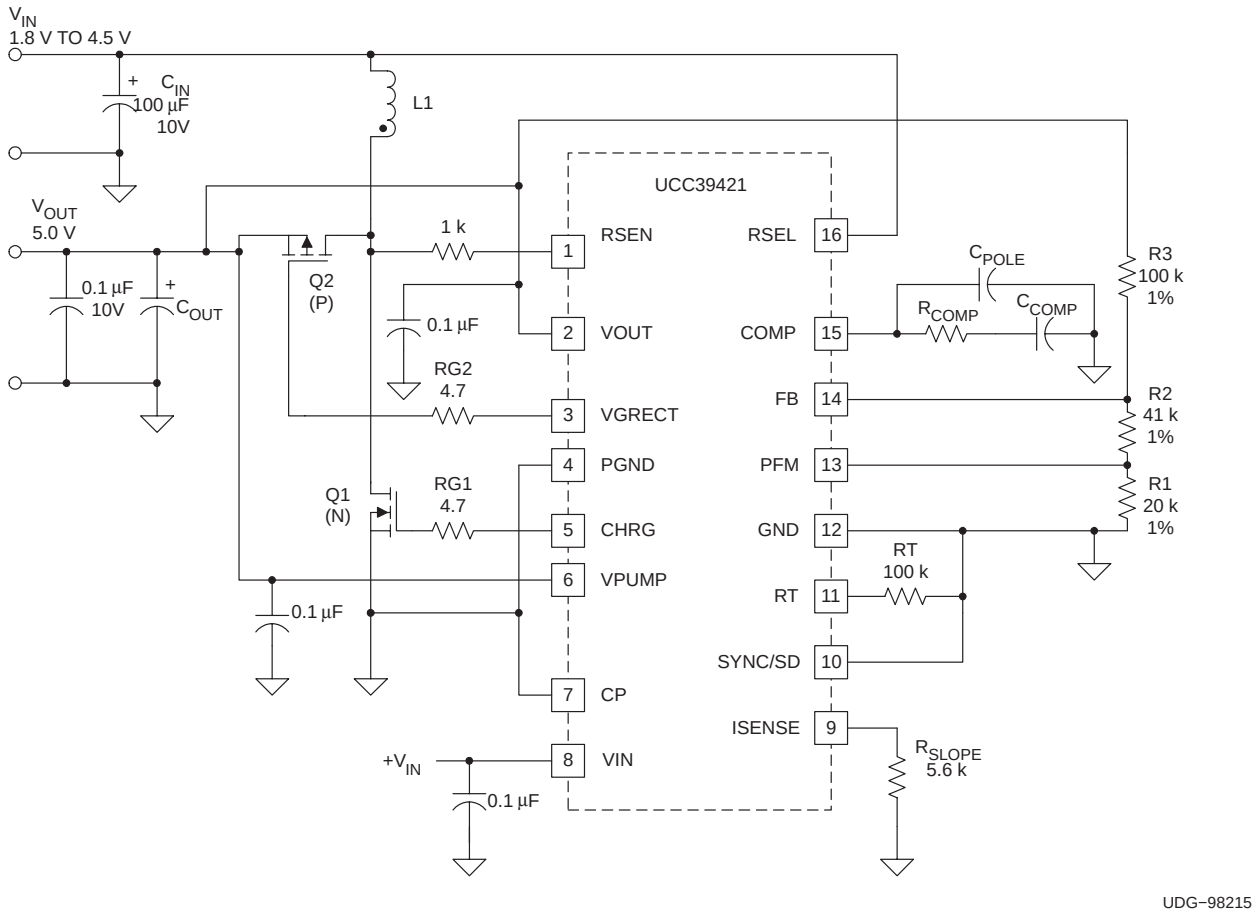


Figure 11. Typical Boost Configuration Using Voltage Mode Control

start up

The UCC39421 incorporates a unique feature to help it start-up at low input voltages. If the input voltage is below 2.5 V at start-up, a separate control circuit takes over until V_{OUT} or V_{PUMP} gets above 2.5 V. In this mode, the charge MOSFET is turned on for 5 µs, or until the voltage on the ISENSE pin reaches 36 mV, whichever occurs first. The charge MOSFET then remains off for a fixed time of 2.5 µs, and the body diode of the synchronous rectifier MOSFET is used to supply current to the output. This cycle repeats until either V_{OUT} or V_{PUMP} exceeds 2.5 V. This results in constant off time control, with a minimum switching frequency of approximately 120 kHz. During this low voltage start-up mode, all other internal circuitry is off, including the synchronous rectifier drive and the slope compensation current source. The peak inductor current during this mode is limited to:

$$I_{PEAK} = \frac{0.036}{R_{SENSE}} \quad (16)$$

APPLICATION INFORMATION

start up (continued)

If input voltages below 2.5 V are expected, it is important to use a low voltage logic N-channel MOSFET (with a threshold voltage around 1 V or less) to ensure start-up at full load.

A block diagram of the low voltage start-up logic is shown in Figure 12.

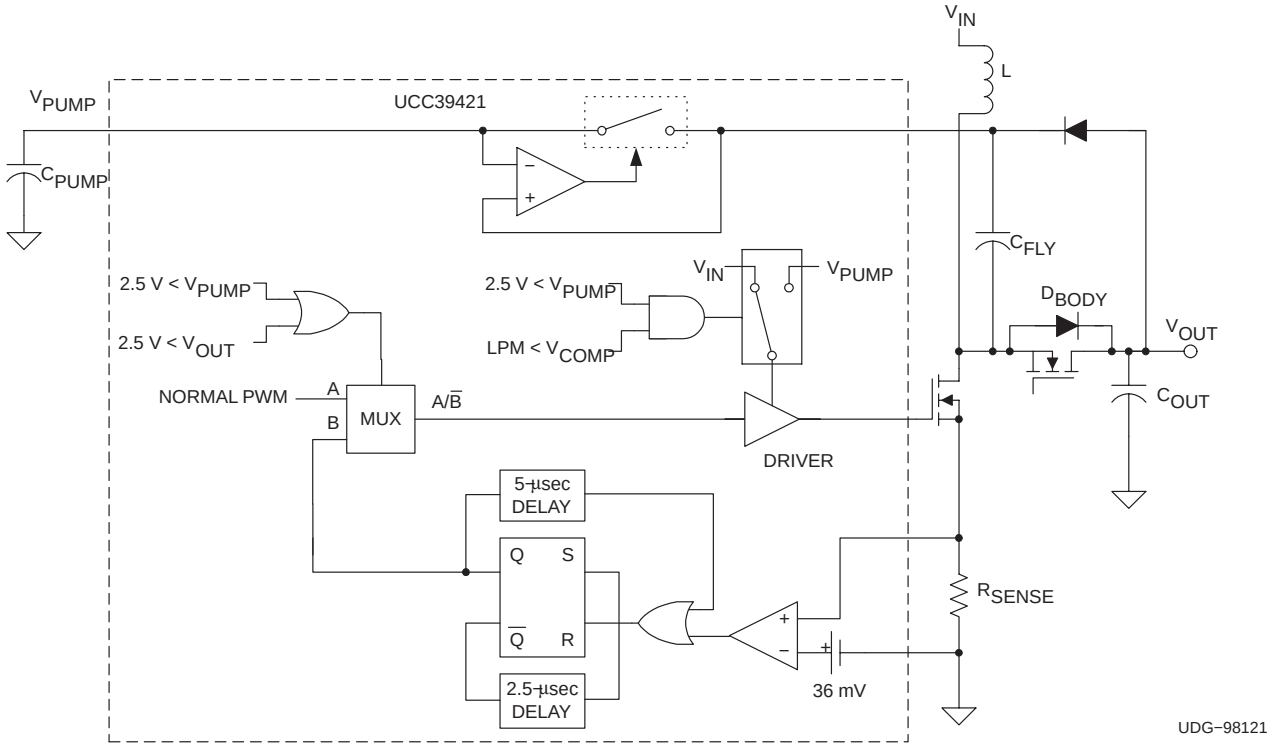


Figure 12. Symplified Diagram of Low Voltage Start−Up and Charge Pump Control Logic

anticross-conduction and adaptive synchronous rectifier commutation logic

When operating in the continuous conduction mode (CCM), the charge MOSFET and the synchronous rectifier MOSFET are simply driven out of phase, so that when one is on the other is off. There is a built-in time delay of about 30 ns to prevent any cross-conduction.

In the event that the converter is operating in the discontinuous conduction mode (DCM), the synchronous rectifier needs to be turned off sooner, when the rectifier current drops to zero. Otherwise, the output begins to discharge as the current reverses and goes back through the rectifier to the input. (This obviously cannot happen when using a conventional diode rectifier). To prevent this, the UCC39421 incorporates a high-speed comparator that senses the voltage on the synchronous rectifier (using the RSEN input) for purposes of commutation. In the boost and SEPIC topologies, the synchronous rectifier is turned off when the voltage on the RSEN pin goes negative with respect to V_{OUT}. For this reason, it is important to have the VOUT pin well decoupled.

APPLICATION INFORMATION

anticross-conduction and adaptive synchronous rectifier commutation logic (continued)

In the flyback topology however (using a ground referenced N-channel MOSFET rectifier), the rectifier voltage is sensed on the MOSFET drain, with respect to ground rather than V_{OUT}. The voltage polarity in this case is opposite that of the boost and SEPIC topologies. This problem is solved with the adaptive logic within the UCC39421. During each charge cycle, while the N-channel charge FET is on, a latch is set if the voltage on the RSEN pin exceeds $V_{IN}/2$. This indicates a flyback topology, since this node is be equal to or greater than V_{IN} at this time. In the case of the boost and the SEPIC, the voltage at the RSEN input is near or below ground, and the latch is not be set. This allows the UCC39421 to sense which topology is in use and adapt the synchronous rectifier commutation logic accordingly. Note that the RSEN input must have a series resistor to limit the current when going below ground. Values less than or equal to 1 kΩ are recommended to prevent time delay due to stray capacitance.

current-sense amplifier and leading edge blanking

The UCC39421 includes a high-speed current-sense amplifier with a nominal gain of 10 to minimize losses associated with the current-sense resistor. The amplifier was designed to provide good response and minimal propagation delay, allowing switching frequencies at 2 MHz. The current-sense resistor should be chosen to provide a maximum peak voltage of 100 mV at full load, with the minimum input voltage.

A leading-edge blanking time of 40 ns is provided to filter out leading-edge spikes in the current-sense waveform. In most applications, this eliminates the need for a filter capacitor on the ISENSE pin.

overcurrent protection

The UCC39421 includes a peak current limit function. If the voltage on the ISENSE pin exceeds 0.15 V after the initial blanking period, the pulse is terminated and the charge MOSFET is turned off.

sync/shutdown input

The SYNC/SD pin has two functions; it may be used to synchronize the UCC39421's switching frequency to an external clock, or to shutdown the IC entirely. In shutdown, the quiescent current is reduced to just a few microamps.

To synchronize the internal clock to an external source, the SYNC/SD pin must be driven high, above 2.0 V minimum. The circuitry syncs to the rising edge of the input, the pulse width is not critical.

To shutdown the converter, the SYNC/SD pin must be held high (above 2.0 V) for a minimum of 29 μs.

This pin should be grounded if not used.

changing the low power mode threshold

For some applications the user may want to lower the low power (LP) mode threshold, or even eliminate this feature altogether. For example, if a boost topology is being used, and the input voltage is below 2.5 V, the gate drive to the charge FET may want to be derived from the pump (or output) voltage under all load conditions, rather than from V_{IN}. This means the converter would never be allowed to operate in LP mode.

APPLICATION INFORMATION

changing the low power mode threshold (continued)

Although the LP mode threshold is internally fixed at 0.6 V (referenced to the pin), the point at which the LP mode is entered can be easily modified by adding a single resistor, as shown in Figure 13. Resistor R_{BIAS} forms a divider with R_{SLOPE} (used for slope compensation) and adds a dc offset to the current-sense input, raising the output voltage of the sense amplifier and *fooling* the LP mode comparator into thinking the load is higher than it is. The required bias resistor to transition out of LP mode for a given peak current can be calculated using the following equation:

$$R_{BIAS} = \frac{R_{SLOPE} \times V_{OUT}}{0.03 - I_{PEAK} \times R_{SENSE}} \quad (17)$$

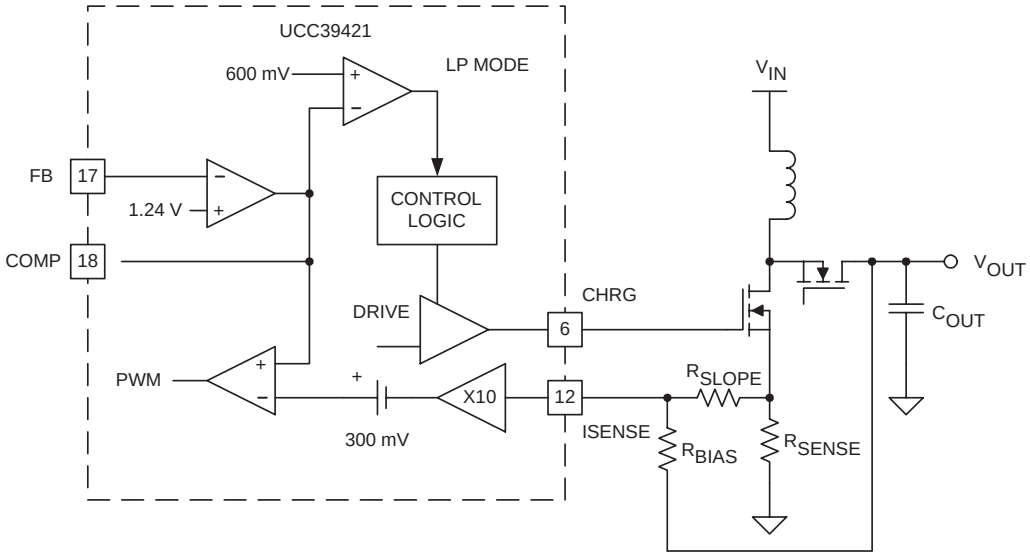


Figure 13. Modifying Low Power (LP) Mode Threshold

Due to the current-sense amplifier gain of 10 and the internal offset of 300 mV, an offset of just 30 mV or more at the ISENSE pin inhibits the LP mode altogether. Note that inhibiting LP mode does not prevent PFM from working, as long as the PFM pin is set to a voltage higher than:

$$\left(10 \times V_{ISENSE}\right) + 0.3V \quad 18)$$

programming the PWM frequency

Some applications may want to remain in a fixed frequency mode of operation, even at light load, rather than going into PFM mode. This lowers efficiency at light load. One way to improve the efficiency while maintaining fixed frequency operation is to lower the PWM frequency under light load conditions. This can be easily done, as shown in Figure 14. By adding a second timing resistor and a small MOSFET switch, the host can switch between two discrete frequencies at any time.

APPLICATION INFORMATION

non-synchronous boost for higher output voltage applications

The UCC39421 can also be used in non-synchronous applications to provide output voltages greater than 8 volts from low voltage inputs. An example of a 12-V boost application is shown in Figure 16. Since none of the IC pins are exposed to the boosted voltage, the output voltage is limited only by the ratings of the external MOSFET, rectifier, and filter capacitor. At these higher output voltages, good efficiency is maintained since the rectifier drop is small compared to the output voltage. Note that PFM mode can still be used to maintain high efficiency at light load. Typical efficiency causes are shown in Figure 15.

Since all the power supply pins (VIN, VOUT, VPUMP) operate off the input voltage, it must be >2.5 V and high enough to assure proper gate drive to the charge FET.

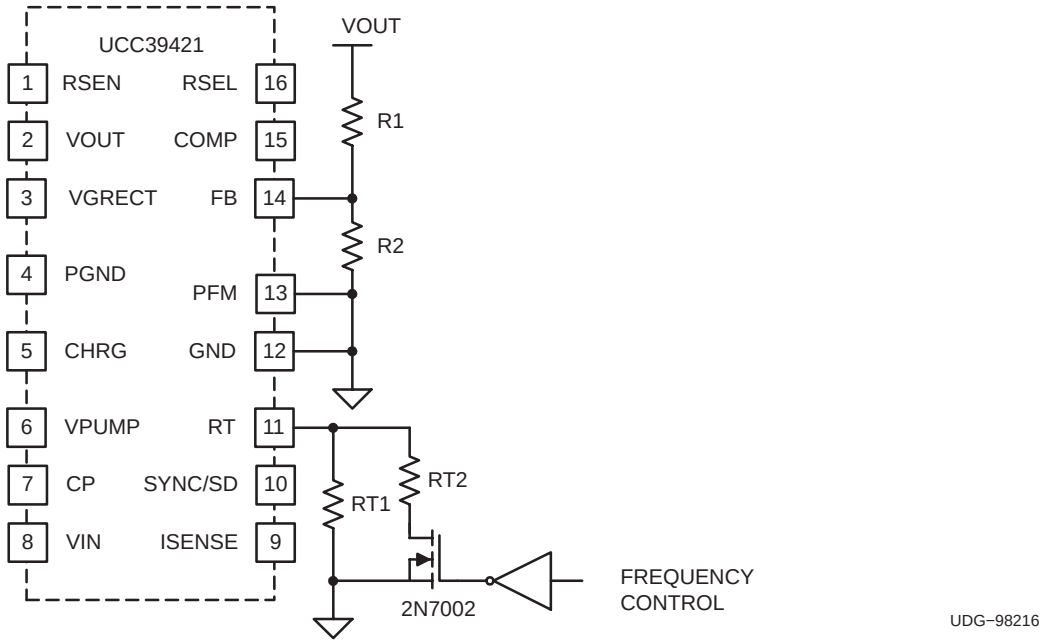


Figure 14. Changing the PWM Frequency

APPLICATION INFORMATION

non−synchronous boost for higher output voltage applications (continued)

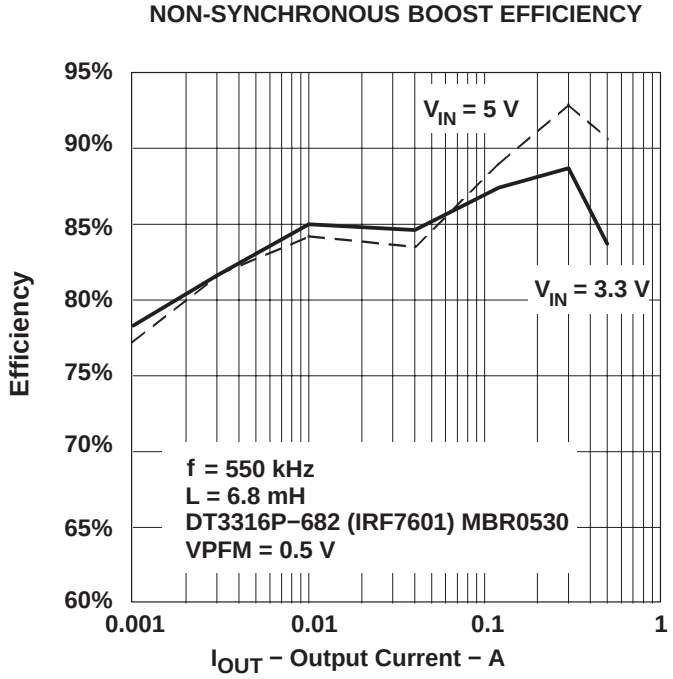


Figure 15

APPLICATION INFORMATION

non−synchronous boost for higher output voltage applications (continued)

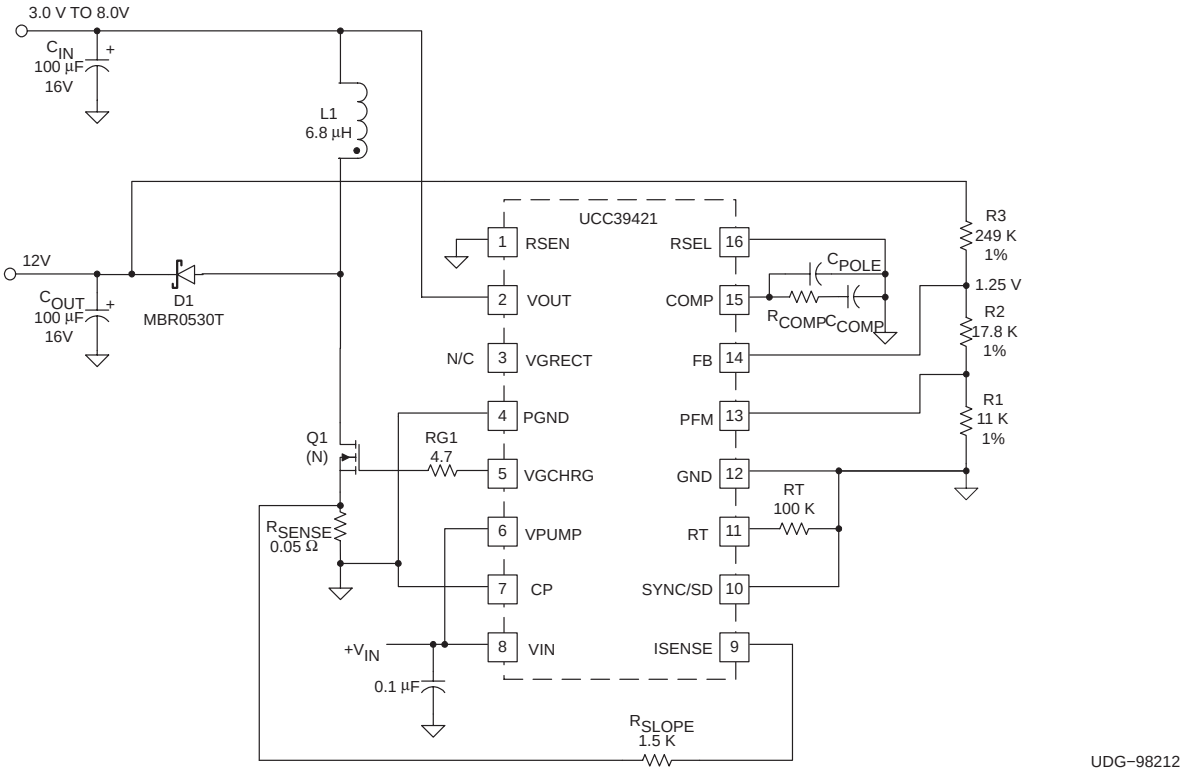


Figure 16. Non-Synchronous Boost Converter for Higher Output Voltages

UCC39422 features

The UCC39422 is a 20-pin device that adds a reset function and an uncommitted comparator to the UCC39421. A simplified diagram of the reset circuit is shown in Figure 17.

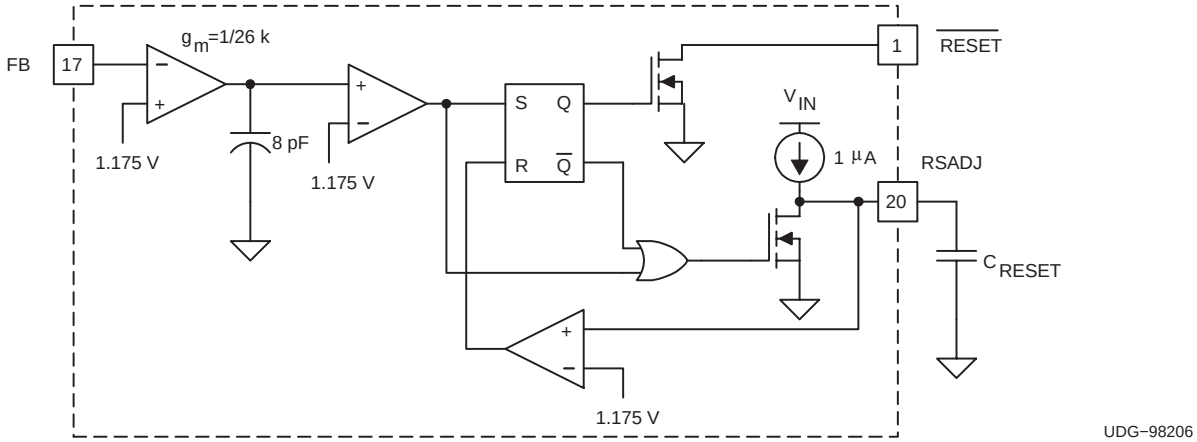


Figure 17. Reset Circuitry

APPLICATION INFORMATION

The reset circuit monitors the voltage at the feedback (FB) pin and issues a reset if the feedback voltage drops below 1.175 V. This represents a 6% drop in output voltage. Monitoring the voltage internally at the FB pin eliminates the need for another external voltage divider. The RESET output is an open-drain output that is active low during reset. It stays low until the feedback voltage is above 1.175 V for a period of time called the reset pulse width, which is user programmable. An external capacitor on the RSADJ pin and an internal 1-μA current source determine the reset pulse width, according to the following equation:

$$t_{RESET} = C_{RESET} \times 1.18 \quad (19)$$

where t_{RESET} is the reset pulse width in seconds, and C_{RESET} is the capacitor value in microFarads (μF).

An adaptive glitch filter is included to prevent nuisance trips. This is implemented using a gm amplifier to charge an 8-pF capacitor to 1.175 V before declaring a reset. This provides a delay which is inversely proportional to the magnitude of the feedback voltage error. The delay time is approximated by the following equation:

$$t_{DELAY} \cong \frac{0.25}{1.175 - V_{FB}} \quad \mu s \quad (20)$$

where t_{DELAY} is the filter delay time in microseconds. Note that the maximum current from the gm amplifier is limited to 2 μA, limiting the minimum time delay to 4.8 μs.

A typical application schematic using the UCC39422 is shown in Figure 18. In this example, R1 and R2 have been selected to trip the LOWBAT output when V_{IN} drops below 2.0 V. Note that the $\overline{\text{RESET}}$ and LOWBAT outputs are open drain and require a pullup.

APPLICATION INFORMATION

UCC39422 features (continued)

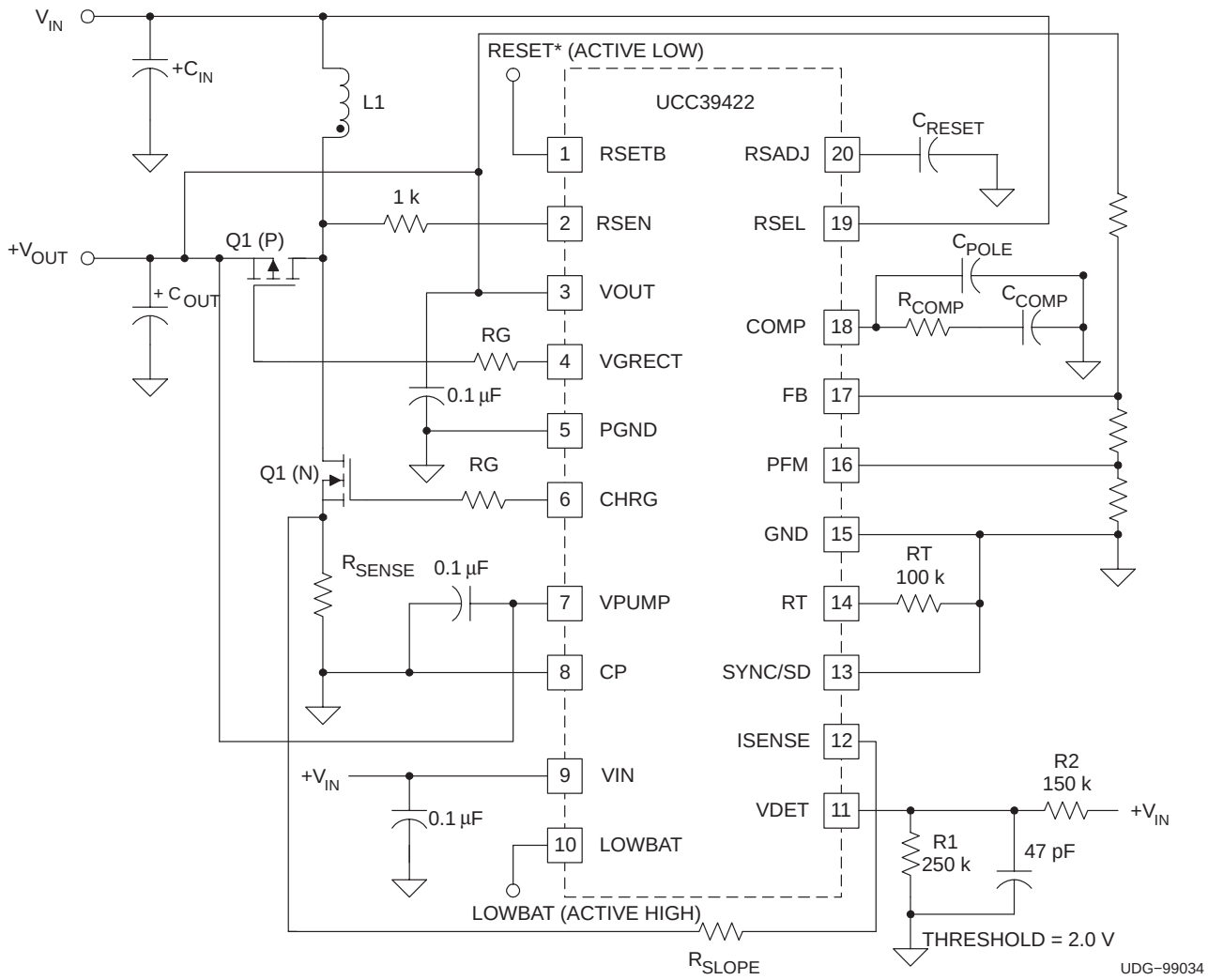


Figure 18. Typical UCC39422 Application

APPLICATION INFORMATION

selecting the inductor

The inductor must be chosen based on the desired operating frequency and the maximum load current. Higher frequencies allow the use of lower inductor values, reducing component size. Higher load currents require larger inductors with higher current ratings and less winding resistance to minimize losses. The inductor must be rated for operation at the highest anticipated peak current. Refer to equation (8) and equation (12) to calculate the peak inductor current for a boost or flyback design, based on V_{IN}, V_{OUT}, maximum load, frequency, and inductor value. Some manufacturers rate their parts for maximum energy storage in microjoules (μJ). This is expressed by:

$$E = 0.5 \times L \times I_{PEAK}^{2} \quad (21)$$

where E is the required energy rating in microjoules. L is the inductor value in microhenries (μH) (with current applied), and I_{PEAK} is the peak current in amps that the inductor sees in the application. Another way in which inductor ratings are sometimes specified is the maximum volt-seconds applied. This is given simply by:

$$E \times T = \frac{V_{IN} \times D}{f} \quad (22)$$

where ET is the required rating in V-μs, D is the duty cycle for a given V_{IN} and V_{OUT}, and f is the switching frequency in MHz. Refer to equations (7) and (11) to calculate the duty cycle for a CCM boost or flyback converter.

In any case, the inductor must use a low loss core designed for high-frequency operation. High-frequency ferrite cores are recommended. Some manufacturers of off-the-shelf surface-mount designs are listed in Table 3. For flyback and SEPIC topologies, use a two-winding coupled inductor. SEPIC designs can also use two discrete inductors.

Table 3. MT COMMERCIAL INDUCTOR MANUFACTURERS

Coilcraft Inc. · (800) 322−2645.1102 Silver Lake RD, Cary, IL 60013
Coiltronics Inc. · (407) 241−7876 6000 Park of Commerce Blvd, Boca Raton, FL 33487
Dale Electronics, Inc. · (605) 665−9301East Highway 50, Yankton, SD 57078
Pulse Engineering Ltd. · (204) 633−4321300 Keewatin Street, Winnipeg, MB R2X 2R9
Sumida · Voice (65) 296−3388 · Fax (65) 293−3390 Block 996, Bendemeer Rd., #04−05/06 Singapore 33944
BH Electronics · (612) 894−9590 12219 Wood Lake Drive, Burnsville, MN 55337
Tokin America Inc. · (408) 432−8020155 Nicholson Lane, San Jose CA 95134

APPLICATION INFORMATION

selecting the filter capacitor

The input and output filter capacitors must have low ESR and low ESL. Surface-mount tantalum, OSCONs or multilayer ceramics (MLCs) are recommended. The capacitor selected must have the proper ripple current rating for the application. Some recommended capacitor types are listed in Table 4.

Table 4. RECOMMENDED SMT FILTER CAPACITORS

Manufacturer	Part Number	Features
AVX	TPS series	Low ESR tantalum
Kemet	T410 series	Low ESR tantalum
Murata	GRM series	Low ESR ceramic
Sanyo	OSCON series	Low ESR organic
Sprague	591D series	Low ESR, low profile tantalum
	594D series	Low ESR tantalum
Tokin	Y5U, Y5V Type	Low ESR ceramic
Taiyo Yuden	X5R Type	Low ESR ceramic

circuit layout and grounding

As with any high frequency switching power supply, circuit layout, hookup, and grounding are critical for proper operation. Although this may be a relatively low-power, low-voltage design, these issues are still very important. The MOSFET turn-on and turn-off times necessary to maintain high efficiency at high switching frequencies of 1 MHz or more result in high dv/dt and di/dts. This makes stray circuit inductance especially critical. In addition, the high impedances associated with low-power designs, such as in the feedback divider, make them especially susceptible to noise pickup.

layout

The component layout should be as tight as possible to minimize stray inductance. This is especially true of the high-current paths, such as in series with the MOSFETs and the input and output filter capacitors.

The components associated with the feedback, compensation and timing should be kept away from the power components (MOSFETs, inductor). Keep all components as close to the IC pins as possible. Nodes that are especially noise sensitive are the FB and RT pins. Other sensitive pins are COMP and PFM.

grounding

A ground plane is highly recommended. The PGND pin of the UCC39421 should be close to the grounded end of the current-sense resistor, the input filter cap, and the output filter cap. The GND pin should be close to the grounded end of the RT resistor, the feedback divider resistor, the ISENSE capacitor (if used), and the compensation network.

MOSFET gate resistors

The UCC39421 includes low-impedance CMOS output drivers for the two external MOSFET switches. The CHRG output has a nominal resistance of 4 Ω, and the RECT has a nominal resistance of 2 Ω. For high-frequency operation using low gate charge MOSFETs, no gate resistors are required. To reduce high-frequency ringing at the MOSFET gates, low-value series gate resistors may be added. These should be non-inductive resistors, with a value of 2 Ω to 10 Ω, depending on the frequency of operation. Lower values results in better switching times, improving efficiency.

APPLICATION INFORMATION

minimizing output ripple and noise spikes

The amount of output ripple is determined primarily by the type of output filter capacitor and how it is connected in the circuit. In most cases, the ripple is be dominated by the ESR (equivalent series resistance) and ESL (equivalent series inductance) of the capacitor, rather than the actual capacitance value. Low ESR and ESL capacitors are mandatory in achieving low output ripple. Surface-mount packages greatly reduce the ESL of the capacitor, minimizing noise spikes. To further minimize high frequency spikes, a surface mount ceramic capacitor should be placed in parallel with the main filter capacitor. For best results, a capacitor should be chosen whose self-resonant frequency is near the frequency of the noise spike. For high switching frequencies, ceramic capacitors alone may be used, reducing size and cost.

For applications where the output ripple must be extremely low, a small LC filter may be added to the output. The resonant frequency should be below the selected switching frequency, but above that of any dynamic loads. The filter's resonant frequency is given by:

$$f_{RES} = \frac{1}{2\pi\sqrt{L \times C}} \quad (23)$$

Where f is the frequency in Hz, L is the filter inductor value in Henries, and C is the filter capacitor value in Farads. It is important to select an inductor rated for the maximum load current and with minimal resistance to reduce losses. The capacitor should be a low-impedance type, such as a tantalum.

If an LC ripple filter is used, the feedback point can be taken before or after the filter, as long as the filter's resonant frequency is well above the loop crossover frequency. Otherwise, the additional phase lag makes the loop unstable. The only advantage to connecting the feedback after the filter is that any small voltage drop across the filter inductor is corrected for in the loop, providing the best possible voltage regulation. However, the resistance of the inductor is usually low enough that the voltage drop is negligible.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC29421PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		29421	Samples
UCC39421PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		39421	Samples
UCC39421PWTR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	39421	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

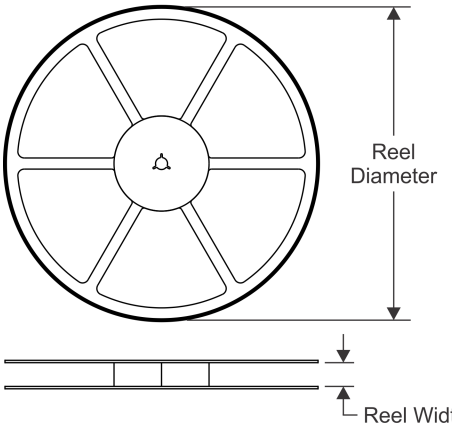
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

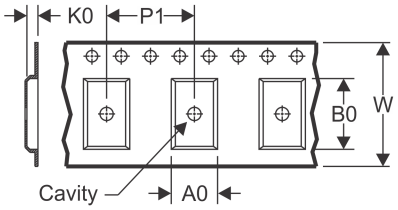
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

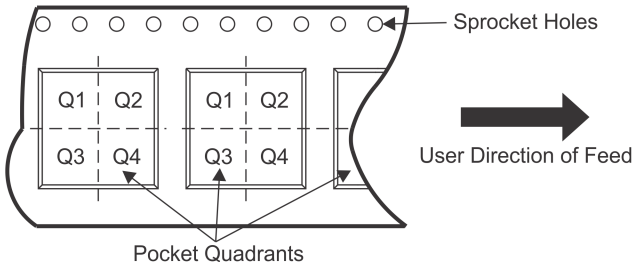


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

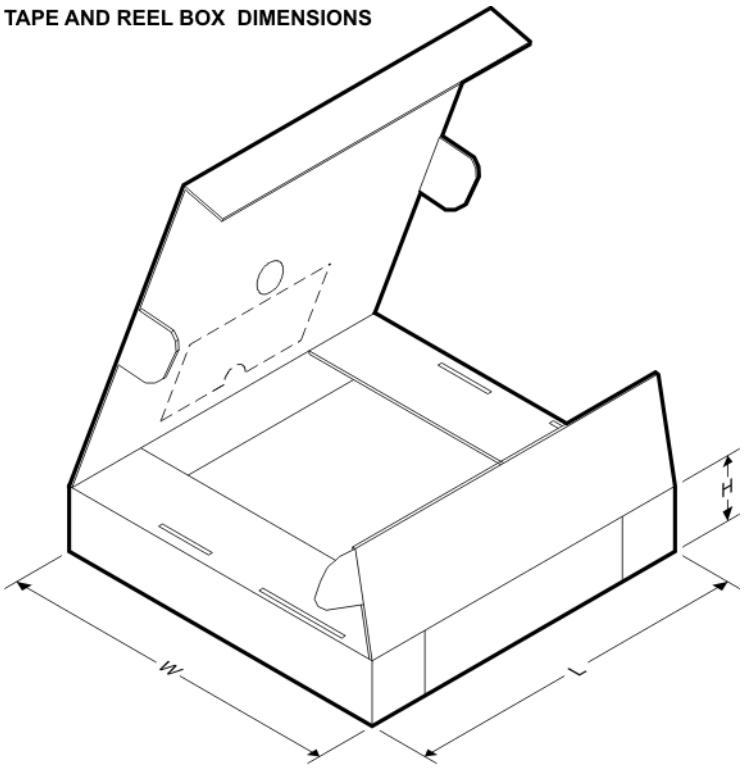
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC39421PWTR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

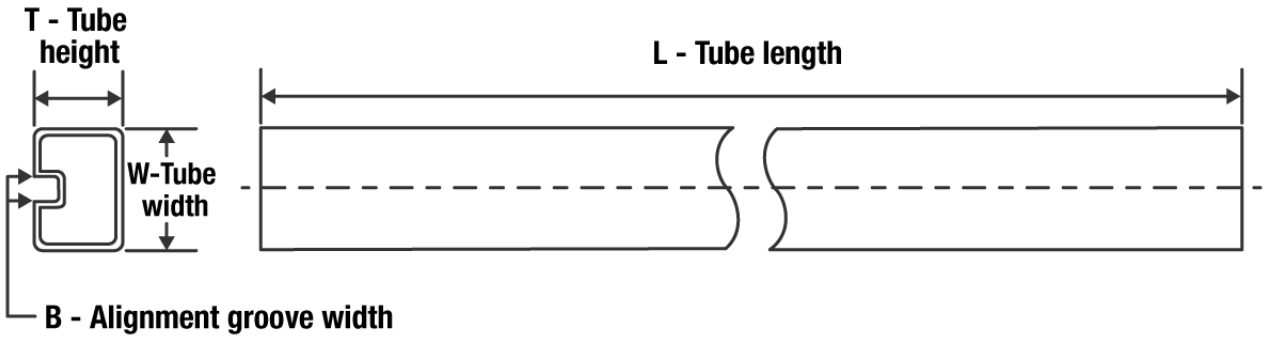
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC39421PWTR	TSSOP	PW	16	2000	853.0	449.0	35.0

TUBE



*All dimensions are nominal

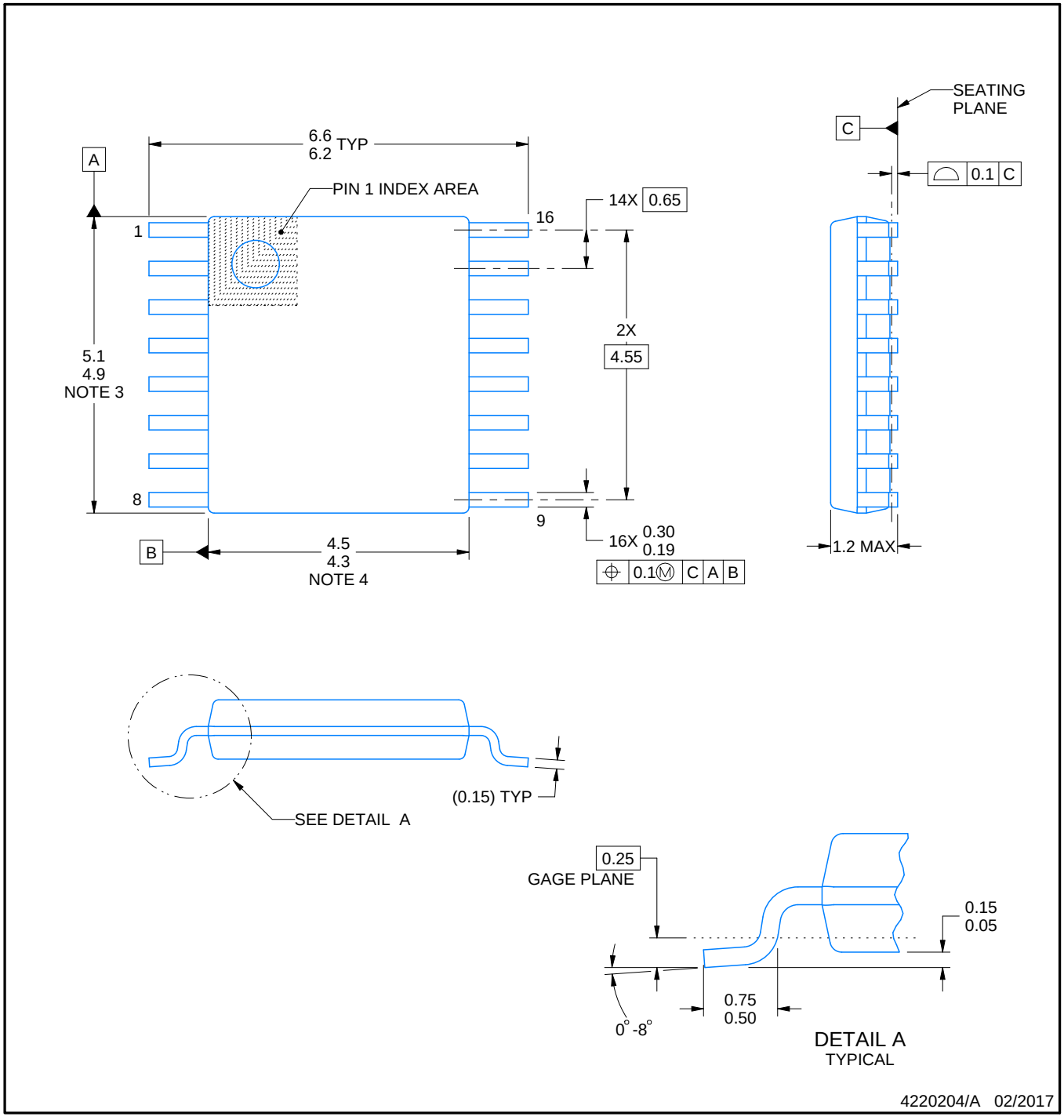
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC29421PW	PW	TSSOP	16	90	530	10.2	3600	3.5
UCC39421PW	PW	TSSOP	16	90	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0016A

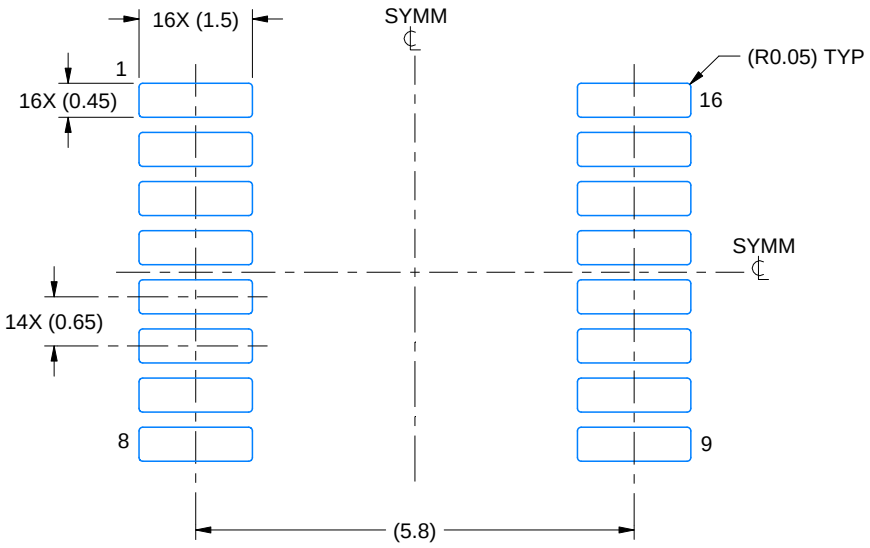
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

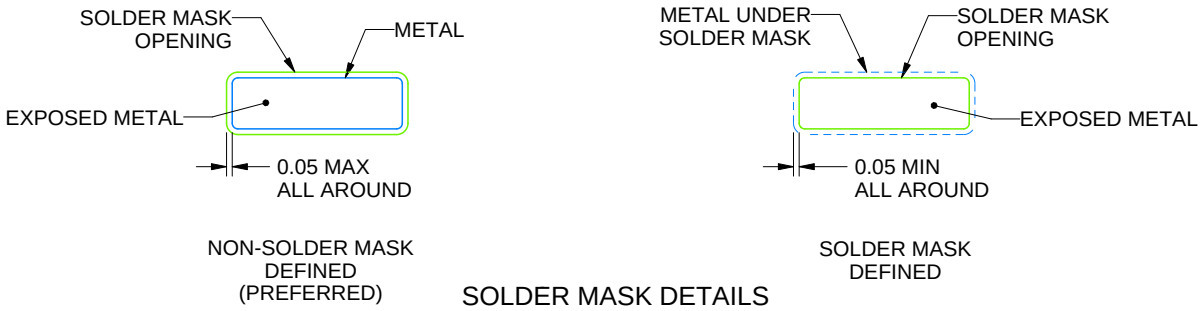


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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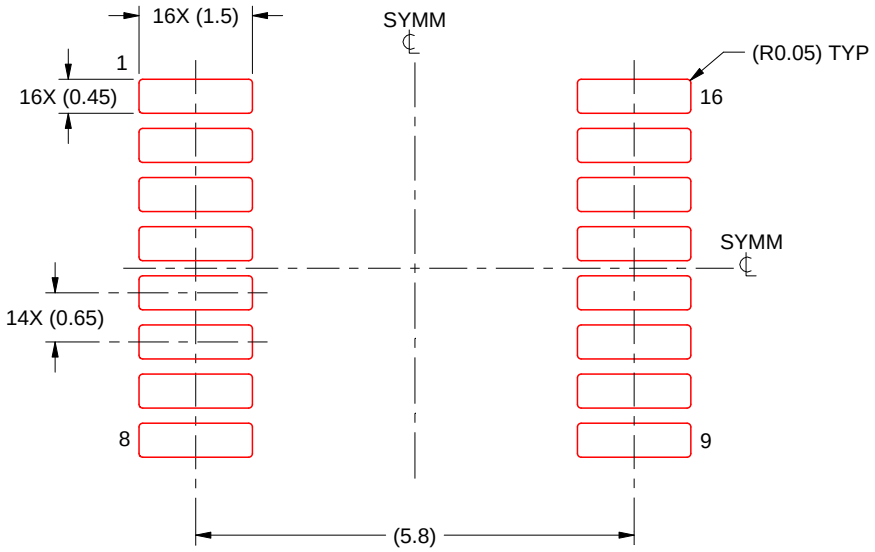
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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